Importance of Thermophysical Properties of Thin Films in ULSICs and Beyond[1]

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ABSTRACT

Ultra Large Scale Integrated Circuits (ULSICs) are fabricated in a single crystal of silicon using submicron device structures arrayed in two dimensions, which are interconnected in the third dimension with multilevel metallizations. The latter use several alternating layers of metal and dielectric films. Currently, 4-level metallizations are used in large volume ULSIC manufacturing. As the technologies advance in ULSICs and beyond, 4-level metallizations are expected to increase to 6-level and higher. In 3-dimensional ICs (3-D ICs) and Ultra Performance ICs (UPICs), in which active devices are also fabricated in the third dimension in addition to the interconnects, the total number of semiconductor, dielectric and metal films increases significantly. The thermophysical properties of all of these films play an ever increasing role in the overall yield, reliability and the chip size of the ICs. The thermophysical properties considered in this paper are the thermal conductivity κ, and the stress σ and its variations on thermal cycling, of the SiO_2 films only. Data of these parameters are shown, with comments on their impact on the reliability of the ICs, as well as the role of Umklapp and point defect scattering mechanisms on the κ of thin films. They are important not only in the current ULSICs for enhanced performance and reliability, but they are even more crucial for the design and manufacturing of the next generation ICs like 3-D and UPICs.

KEY WORDS: electromigration lifetime ; integrated circuits; reliability; SiO_2 films; stresses; thermal conductivity.

1. INTRODUCTION

Currently available Ultra Large Scale Integrated Circuits (ULSICs) have about 5 - 10 million transistors arrayed as densely as allowed by the design rules in 2-dimensions on a single crystal of silicon, which are interconnected by 4-level multilevel metallizations [1]. The key objectives are to obtain the smallest IC chip, with maximum performance, reliability and yield. The multilevel metallizations use alternating layers of aluminum-based alloys having under- and cap-layers of refractory metals, and SiO_2 - based inter-layer-dielectric (ILD) films [2]. The film thicknesses can range from a few hundred to several thousand Angstroms (A°). The thermophysical properties such as thermal conductivity κ and stress σ of these films are important for the reliability of the ULSICs. While the κ and σ of both the metal and ILDs need to be considered, the data of SiO_2 ILDs only will be presented in this paper. The κ of thin SiO_2 films is lower than its value κ_B for bulk quartz. The latter has been widely used for the thermal modelling of the ICs, which will give erroneous values for the electromigration lifetime t_{50} of the interconnects. The stress σ of the ILDs varies on thermal cycling, and its value and type, ie, whether it is compressive or tensile, have an effect on the t_{50} . Knowing and controlling the κ and σ of the ILDs, the performance and the reliability of the ICs can be enhanced.

2. THERMAL CONDUCTIVITY

2.1 Variation with film thickness

The thermal conductivity κ of SiO_2 films used in ULSICs varies with their film thickness, and also with their method of deposition, growth and composition [3]. The measurement technique and the details of the processes used for the various SiO_2 films, have been given earlier [3]. Fig. 1 shows the measured values of κ for these SiO_2 films vs

their film thicknesses t_{ox} . The various processes used for the SiO_2 films were thermal growth (Thermal), plasma enhanced CVD for undoped (PTEOS and SiH_4), phosphorus doped (PSG), boron + phosphorus doped (BPSG), and a non-plasma O_3 assisted CVD of TEOS (O_3 -TEOS) for undoped films. The thermal conductivity of bulk fused quartz κ_B is also shown in Fig. 1, which is independent of "film thickness" and its value in the units chosen is 14 mW/cm C. As it is clear from the data of Fig. 1, the κ values of the various SiO_2 films are lower than κ_B , they decrease with decreasing film thicknesses t_{ox} , and they vary with the process used for their deposition. When the κ values were plotted for the various SiO_2 films vs their respective $1/ t_{ox}^{1/2}$, a linear behavior was observed for all the films. This is shown in Fig. 2 for the thermal, PTEOS and the annealed PTEOS-a films only. Such a linear behavior is predicted by the model of Savvides and Goldsmid [4].

2.2 Annealing effects and diagnostics for film quality

As mentioned in the previous section 2.1, the experimental κ data of various types of SiO_2 films vs $1/t_{ox}^{1/2}$ fit their respective straight lines. When they are extrapolated to the origin of abscissa, ie, at $1/t_{ox}^{1/2} = 0$, their intercept on the ordinate gives κ_o, which is the "extrapolated bulk thermal conductivity", for each film respectively. The details of the data and analyses are given in reference [3]. However, Fig. 2 shows that the κ_o for the annealed PTEOS film is greater than that for the as-deposited PTEOS film. This is because of the densification of the PTEOS film due to annealing. It was also observed that the κ_o of the thermally grown SiO_2 film is the highest (13.6) of all the SiO_2 films studied, and that it was closest to the bulk quartz value $\kappa_B = 14$. Thus, the experimentally measured κ_o of a film can be used as a diagnostics for the SiO_2 film quality, and for the reproducibility of the process used for its manufacturing.

2.3 Diagnostics for adhesion

The number of films used in the manufacturing of ULSIC's is ever increasing, and is expected to continue to increase as the technologies advance. The adhesion of each film during the manufacturing processes, eg, photoresist, ILDs and multilevel metal films, and in the finished ULSIC product, is absolutely crucial for their yield and reliability. No quantitative technique to characterize and monitor adhesion, in particular in the submicron geometries used in ULSIC manufacturing, had been even proposed what to say of using it in practice, until recently [5]. The slope, s , of the straight line of Fig. 2 is related to the mean free relaxation times for Umklapp phon scattering, τ_U , and for phonon scattering by point defects in the material of the film, τ_{PD} . The τ_{PD} is related to its bulk and surface scattering components, the latter being dependent on the adhesion of the film to the surface. A model was proposed [5] which gives s as the parameter to characterize adhesion quantitatively for a given film and its manufacturing process. The value of s decreases as the film adhesion gets better. As an example, Fig. 2 shows that the s of the annealed PTEOS film, PTEOS-a, is lower than for the same as-deposited film, which is of course due to the improvement of adhesion on annealing. Analyses similar to that given in reference [5] need to be extended for characterizing other films used in ULSIC manufacturing.

2.4 Impact on reliability

Two aspects of reliability shall be addressed here, viz, electromigration lifetime, t_{50} , of aluminum based interconnects (AlX), and adhesion of films. The t_{50} depends exponentially on the temperature of AlX interconnects [6] used in the multilevel metallizations of ULSICs. The increase in temperature during the use and/or accelerated testing of the ULSICs is inversely proportional to the thermal conductivity of the ILDs, and it is directly proportional to the interconnect metal resistivity and thickness, the

thickness of the ILDs, and the square of the current density being used in the interconnects [7]. Thus for a given structure of multilevel metallizations and the use conditions in the ULSICs, the lower the thermal conductivity of the ILD, the lower would be the t_{50} . When the bulk thermal conductivity value κ_B is used in the thermal modelling, the t_{50} value calculated will be higher than the actual value of t_{50} which will be obtained with the true values of κ corresponding to the thicknesses of the ILDs in the ULSIC. Therefore, a user of the ULSIC can have a misleading information on its reliability. To enhance the reliability, proper attention needs to be paid to the thermal conductivity and the other parameters of the ULSIC films.

The adhesion of the various films needs to be good during and after the processing of the ULSICs. The measurement of the slope *s* defined in section 2.3, using microminiature test devices having submicrom geometries such as those of the ULSICs, provides the quantitative characterization of adhesion during and after normal and accelerated testing of the ULSICs. Thus for a given film-interface, minimum vaue of *s* and maintaining its constant value, will give the highest reliability.

3. STRESSES

Stresses of all the films used in the ULSICs are important for its yield, reliability and performance. However, the stress behavior of only SiO_2 ILDs shall be discussed in this paper. For details, see references [8] and [9].

3.1 Variation with post-metal-1 thermal recycling

Post-metal-1 thermal recycling is defined as the temperature range, through which the ULSIC wafers are subjected to, should not exceed about 450 °C. This is to prevent the interaction of AlX metallizations with Si. As shown in [8], an ILD having an initial small compressive stress, ends up with a high tensile stress after the post-metal-1 thermal

recycling. A simplified explanation for such a behavior is that the "SiO_4" tetrahedra in the ILD do not get sufficient energy in this thermal regime to re-configure themselves.

3.2 Variation with pre-metal-1 thermal recycling

Pre-metal-1 thermal recycling is defined as the temperature range, through which the ULSIC wafers are subjected to, is in excess of 450 °C, usually up to about 950 °C. Higher temperatures can be reached in this recycling, because no metal has been deposited yet on the ULSIC wafers. Again as shown in [8], an ILD having an initial small compressive stress, ends up with a slightly higher compressive stress after the pre-metal-1 thermal recycling. A simplified explanation for such a behavior is that the "SiO_4" tetrahedra in the ILD do get sufficient energy in this thermal regime to re-configure themselves.

3.3 Stress type and reliability

It has been shown [9] that the stress type in the ILD has a significant effect on the electromigration lifetime, t_{50} , of AlX interconnects. The effect of the stress type, ie, whether it is compressive or tensile, manifests itself in the residual resistivity of the AlX. Fig. 3 shows the variation of AlX resistance vs. temperature for three cases: one with tensile ILD; second with compressive ILD; third without any ILD, ie, unpassivated [9]. The residual resistivity behavior regime is observed at temperatures < 40 °K. The value of the residual resistivity is observed to be highest for an AlX interconnect with an ILD having a compressive stress, it is lower with an ILD having a tensile stress, and it is lowest when no ILD is used, ie, when the AlX interconnect is unpassivated. A model to explain this behavior has been given earlier [10]. The significance of all this is, that all the interconnects being currently used in the ULSICs are AlX-based, and they are all passivated with SiO_2 -based ILDs. It has been shown [9, 10] that the t_{50} of AlX interconnects is approximately 100% higher with ILDs having tensile stress as compared to those having

compressive stress. To get the highest t_{50} in a given multilevel metallization structure of ULSIC, and achieve the highest reliability, further work is necessary to optimize the parameters of the stress values, types, thicknesses, processes, etc. A quantitative electrical characterization technique to monitor the quality and the reliability of AlX metallizations has been also proposed based on the above work [9, 10]. Its use in ULSIC manufacturing appears quite promising.

4. SUMMARY

It has been shown that the thermophysical properties of thin films, eg, thermal conductivity, κ, and the stress, σ, are important parameters which need to be understood, and used in the IC process and layout design, better in the current ULSICs for enhanced performance and reliability, and that they are even more important for the next generation ICs such as 3-D and UPICs. The κ of SiO_2 ILD films is lower than its value for bulk quartz, it decreases with decreasing film thickness, and it varies with the process used for its deposition. A quantitative technique to monitor the quality of the ILD films, has been given which uses the extrapolated value of κ as an effective bulk quartz parameter for the process used for the ILD. Further, a quantitative technique to monitor the adhesion of films has been given, which uses the slope s of κ vs. $1/t_{ox}^{1/2}$ straight line. Lowest value of s signifies the best adhesion. This technique is the only technique which allows monitoring of adhesion of films in submicron geometries used in ULSICs, during and after normal and accelerated electrical testing. It has been also shown that the stress of ILD films has an important effect on the reliability of ULSICs. A quantitative electrical technique has been given to characterize and enhance the reliability of ULSICs.

REFERENCES

1. *P-6 Processor* , Intel Corporation (1995).

2. A. N. Saxena, *VMIC State-of-the-Art Seminar* , p.8 (1989); A. N. Saxena, K. Ramkumar, S. K. Ghosh and M. A. Bourgeois, *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)* , Minneapolis, MN, p.12 (1993).

3. A. N. Saxena and M. Bourgeois, *Proc. 11th International VMIC* , p. 126 (1994).

4. N. Savvides and H. J. Goldsmid, *Physics Letters* , **41A** (13), 193 (1972).

5. A. N. Saxena, *Mittal Festschrifft*, W. J. van Ooij and H. R. Anderson, Jr, eds (VSP International Science Publishers, Zeist, The Netherlands, 1997), p. 1.

6. J. R. Black, *IEEE Proc. IRPS* , p. 300 (1982).

7. H. A. Schafft, *IEEE Trans. on Electronic Devices* , **ED-34**, 3 (1987).

8. K. Ramkumar and A. N. Saxena, *J. Electrochemical Soc.* **139**, 1437 (1992).

9. A. N. Saxena, K. Ramkumar and S. K. Ghosh, *Proc. 11th International VMIC* , p. 252 (1994).

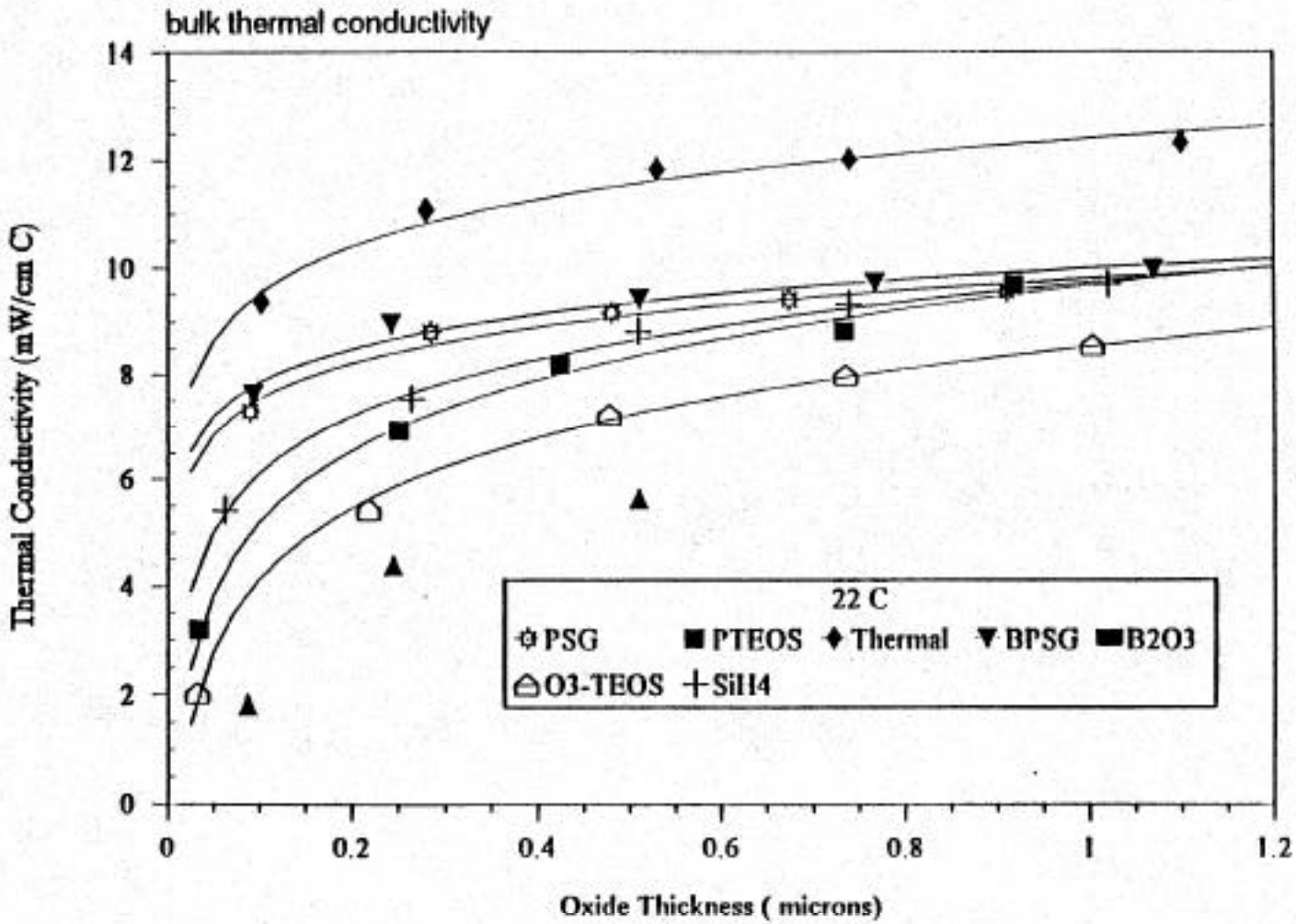
10. A. N. Saxena, *Proc. 12th International VMIC* , p. 430 (1995).

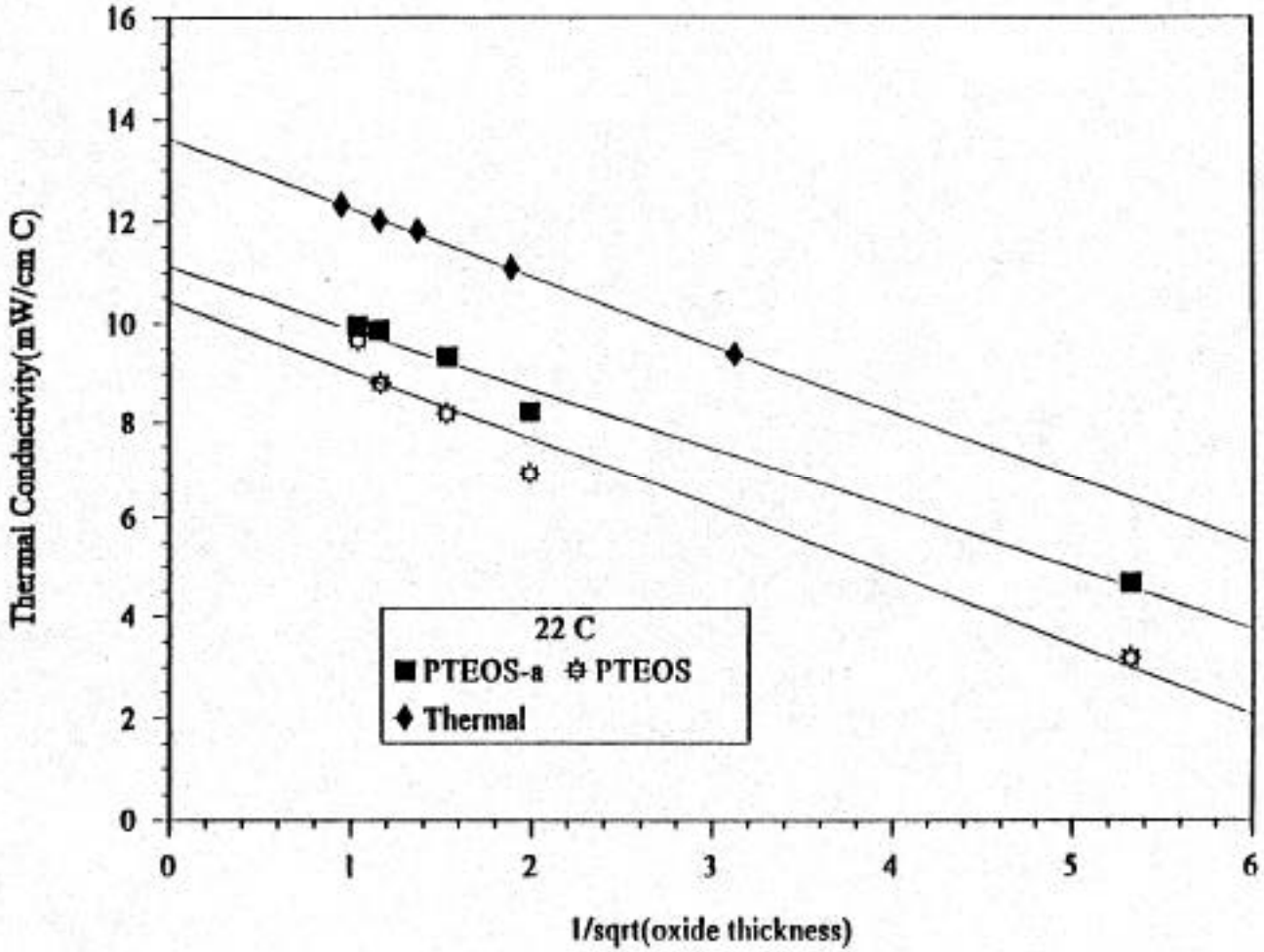
FIGURE CAPTIONS

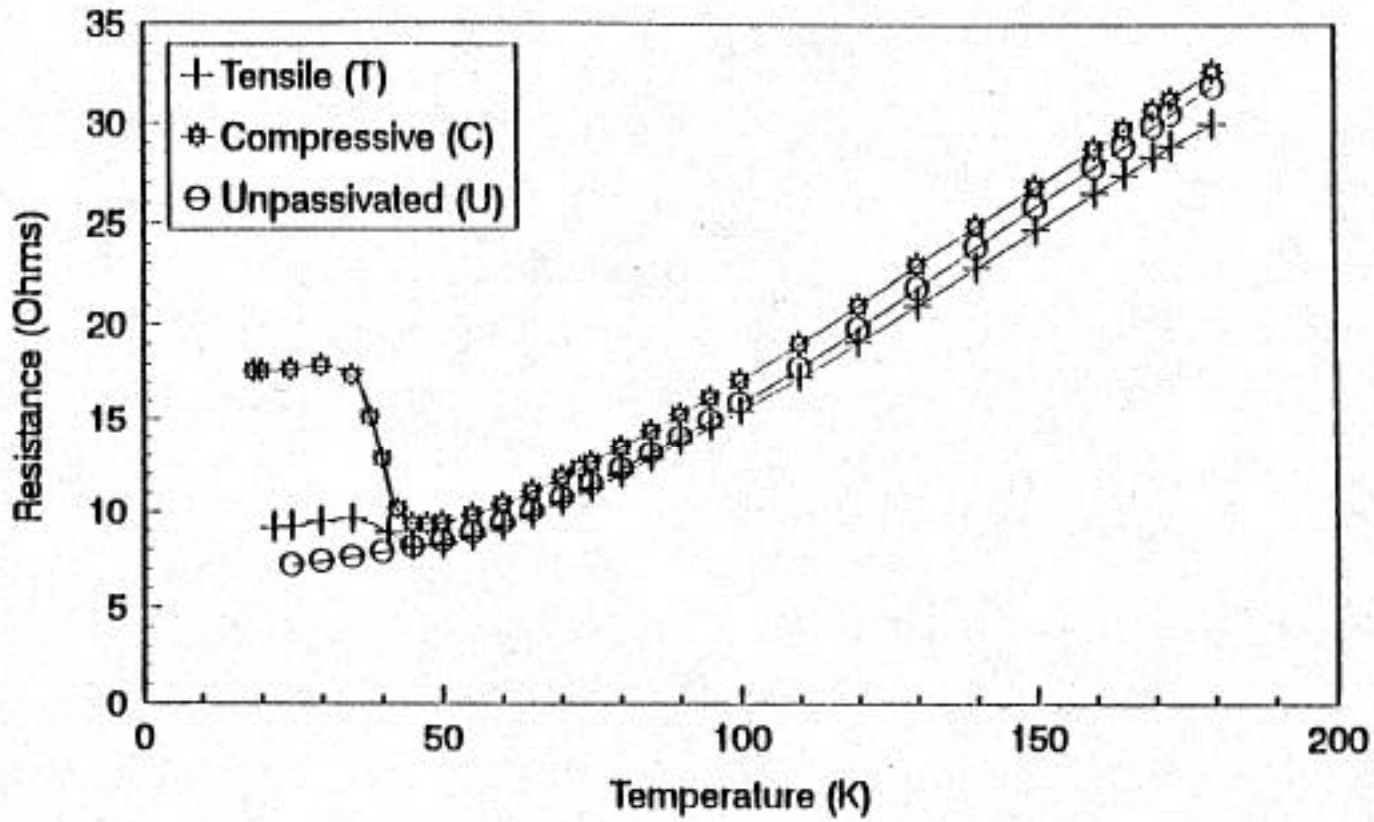
Fig. 1. Thermal conductivity of PSG, PTEOS, Thermal, BPSG, SiH_4 , O_3-TEOS oxides at 22 °C vs. oxide thickness.

Fig. 2. Thermal conductivity of as-deposited, annealed PTEOS and Thermal oxides at 22 °C vs $1/ t_{ox}^{1/2}$.

Fig. 3. R vs T for AlX interconnects without and with tensile and compressive ILD's.


bulk thermal conductivity
Thermal Conductivity (mW/cm C)
Oxide Thickness (microns)
22 C
PSG
PTEOS
Thermal
BPSG
B2O3
O3-TEOS
SiH4
0
2
4
6
8
10
12
14
0
0.2
0.4
0.6
0.8
1
1.2


16
14
12
10
8
6
4
2
0
Thermal Conductivity(mW/cm C)
0
1
2
3
4
5
6
1/sqrt(oxide thickness)
22 C
PTEOS-a
PTEOS
Thermal


Tensile (T)
Compressive (C)
Unpassivated (U)
Resistance (Ohms)
Temperature (K)
0
5
10
15
20
25
30
35
0
50
100
150
200