

# Electric Current Induced Thermomechanical Fatigue Testing of Interconnects

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**Abstract.** We demonstrate the use of electrical methods for evaluating the thermomechanical fatigue properties of patterned aluminum and copper interconnects on silicon-based substrates. Through a careful selection of alternating current frequency and current density, we used controlled Joule heating to simulate in an accelerated manner the type of low frequency thermal stress cycles that an interconnect structure may undergo. Sources of such stressing may include power cycling, energy-saving modes, or application-specific fluctuations, as opposed to stressing at chip operating frequencies. The thermal stresses are caused by differences in thermal expansion properties between the metal and constraining substrate or passivation. Test conditions included a frequency of 100 Hz and current density of 11 – 16 MA/cm<sup>2</sup>, which led to a cyclic temperature amplitude of approximately 100 K, and corresponding cyclic stress amplitude in excess of 100 MPa for Al-1Si and Cu lines on oxidized silicon. The failure mechanism differs from that observed in direct current electromigration studies, and involves formation of localized plasticity, which causes topography changes on the less-constrained surfaces of the interconnect. Open circuit eventually took place by melting at a region of severely reduced cross-sectional area. In these studies, both Al-1Si and Cu responded to power cycling by deforming in a manner that was highly dependent upon variations in grain size and orientation. Isolated patches of damage appeared early within the confines of individual grains or clusters of grains, as determined by automated electron backscatter diffraction. With increased cycling or with increased current density, the extent of damage became more severe and widespread. We discuss the utility of electrical methods for accelerated testing of mechanical reliability.

**Keywords:** Electrical testing, electron backscatter diffraction, interconnect reliability, thermomechanical cycling, thermomechanical fatigue, thin film fatigue.

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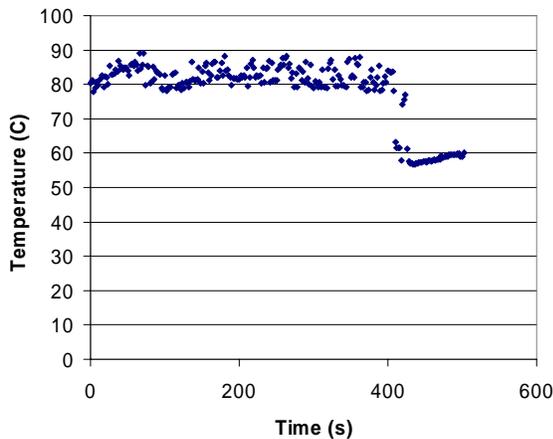
## INTRODUCTION

We describe an electrical test method for measuring mechanical response of thin films and interconnects on silicon substrates. In particular, we address thermomechanical fatigue, using alternating currents running at low frequency. The purpose for developing an electrical method for measuring mechanical response is to circumvent some of the difficulties associated with methods like microtensile testing of free-standing films [1] or nanoindentation of films on substrates [2]. Non-trivial specimen preparation or non-straightforward property extraction tend to render these methods cumbersome in terms of implementation and interpretation.

Thermomechanical fatigue is a reliability concern for any multi-material system that undergoes significant thermal cycling, because of the resulting accumulated strains due to differential thermal

expansion between the materials. Thermal excursions occur during processing steps such as film deposition at high temperature or annealing for relief of internal stress or grain structure stabilization. They can also occur during operation because of power cycling, energy-saving, or even processor-intensive application usage, where maximum cpu temperatures can approach 90 °C, as shown in figure 1. The plot shows temperature versus time, while a processor-intensive application was run, with temperature measured directly on the case of the die. The measurements were made using a diode built in to a late-model commercial desktop computer. A 70 K temperature change leads to a thermal strain of approximately 0.1% and corresponding thermal stresses of 100 MPa for Al on Si and 125 MPa for Cu on Si; these values are similar to thin film yield strengths as measured by microtensile testing. We can make a simple estimate of the number of thermal cycles undergone by interconnects in a normal computer (excluding

excursions encountered during processing) by considering what might be viewed as “typical” operation in a business environment: starting up and shutting down 1 power cycle per day, going into energy-saving mode 10 times per day, and running a cpu-intensive application 10 times per day, resulting in 21 thermal cycles per day, or 5460 cycles in a 260 work-day year. Over the course of a “useful” lifetime of 5 years, this results in 27,300 total thermal cycles.

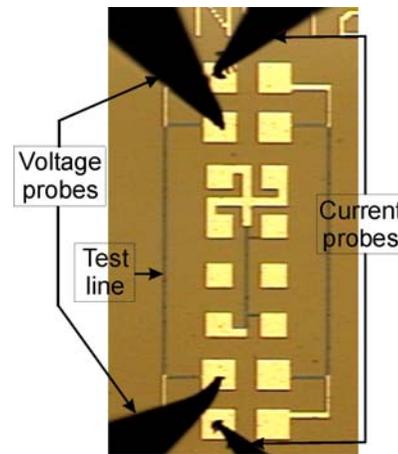


**FIGURE 1.** Computer processor temperature versus time, during operation of a processor-intensive application. The application was terminated at approximately 400 s.

The reliability issue centers on failure initiation following accumulation of strain during cycling. Failures can take the form of resistivity increases due to the introduction of excessive lattice defects [3], brittle film cracking due to deformation of underlying metal films [4], or even open- or short-circuits due to metal deformation [5]. To date, microprocessors have not exhibited significant numbers of failures due to such causes, and we postulate this to be due to the constraining effect of rigid dielectric materials such as  $\text{SiO}_2$ , which suppress surface damage due to cyclic plasticity. However, the incorporation of more compliant dielectrics such as polymeric low- $k$  materials suggests thermomechanical fatigue could become problematic, as plasticity within the metal lines is no longer suppressed by the passivation [5]. A test method for assessing thermomechanical fatigue reliability in an accelerated manner therefore becomes valuable in the design and performance prediction of new interconnect/dielectric systems. Our goal is to develop such a method, and to qualify it by means of rigorous comparison to the reference mechanical testing techniques of microtensile testing and nanoindentation. We report in this paper recent results on AC-induced thermomechanical fatigue of Cu and Al-1Si interconnects.

## EXPERIMENTAL

Most of the AC tests were carried out on non-passivated, single-level structures composed of patterned and etched Al-1Si lines sputtered onto thermally oxidized silicon, using conventional processing parameters. We used a NIST-2 test structure originally designed for electromigration and thermal conductivity measurements. The lines were 800  $\mu\text{m}$  long, 3.3  $\mu\text{m}$  wide, and 0.5  $\mu\text{m}$  thick. Current pads and voltage taps were present at each end of a given line, as shown in Figure 2. We carried out an additional five tests on non-passivated, sputtered Cu lines of length 800  $\mu\text{m}$ , width 2.0  $\mu\text{m}$ , and thickness 0.7  $\mu\text{m}$ .



**FIGURE 2.** Optical microscope image of a NIST-2 test structure with four probes in place for electrical testing.

Testing was conducted on a 4-point probe station using 100 Hz sinusoidal alternating currents with zero DC offset. Current was supplied with a current calibrator, which was driven by an arbitrary waveform generator. The test chip was held in place on a steel stage during testing using a vacuum chuck. Lifetime tests were conducted continuously until the test lines became electrically open. Current was measured with an uncertainty of 0.06 mA, and line cross-sections were measured with an uncertainty of 0.05  $\mu\text{m}^2$ , leading to an uncertainty in current density of 0.3  $\text{MA}/\text{cm}^2$ . Current densities (rms) applied to individual lines ranged from 11 to 16  $\text{MA}/\text{cm}^2$ . Lifetimes to open circuit were determined for all specimens, with an uncertainty of approximately 1 s.

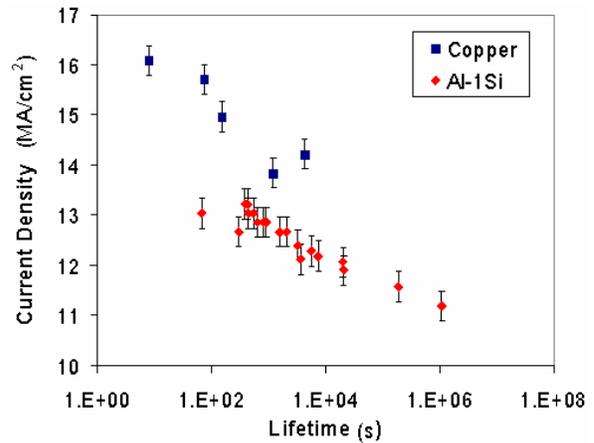
Microstructure evolution during the course of one particular test on an Al-1Si line was monitored using field emission scanning electron microscopy (FE-SEM) and automated electron backscatter diffraction (EBSD). For that particular specimen, a current

density of  $12.2 \text{ MA/cm}^2$  was applied. The average specimen temperature, as monitored using a thermocouple attached directly to the die, indicated a rise of  $< 10 \text{ K}$  during electrical testing. However, the low-frequency AC signals led to temperature cycling superimposed onto the average die temperature, with amplitude of approximately  $100 \text{ K}$ , at a frequency of  $200 \text{ Hz}$  [5], which corresponds to the power cycling input into the line. We collected FE-SEM and EBSD data from the entire line prior to testing, to establish the as-deposited condition. The line was then subjected to testing for  $10 \text{ s}$  and removed from the probe station for another series of EBSD measurements. The line was then subjected to another  $10 \text{ s}$  of testing, and so on. In this manner, we collected FE-SEM and EBSD data after the following accumulated time increments (in seconds):  $0, 10, 20, 40, 80, 160, \text{ and } 320$ . The specimen failed after  $697 \text{ s}$ . EBSD measurements were made using an accelerating voltage of  $15 \text{ kV}$  and electron beam step increments of  $200 \text{ nm}$ . Scan times were typically less than  $5 \text{ minutes}$  for the collection of  $1800$  points with  $8 \times 8$  binning. All EBSD orientation maps are shown in the as-collected state, with no software-imposed filtering or clean-up algorithms applied.

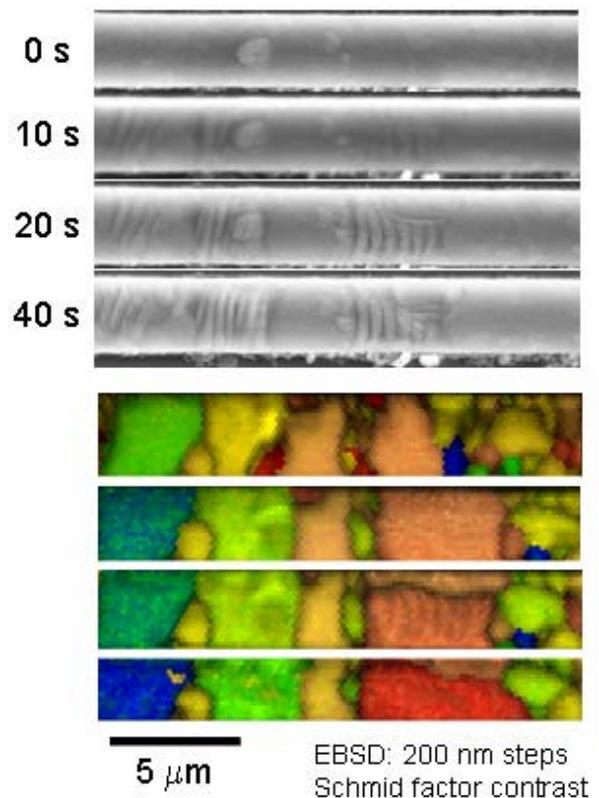
## RESULTS

Figure 3 shows a plot of rms current density against time to open circuit, for both the Al-1Si and Cu lines. The form of this plot follows the convention used in representing stress-controlled fatigue lifetime data, or S-N curves. Namely, we plot the applied stress (current density, in this case) versus the measured lifetime. Despite the limited data obtained from the copper specimens, a trend is apparent in that copper lines are able to withstand higher current densities than Al-1Si lines, for a given lifetime. Further, for a given current density, copper shows increased lifetime.

All specimens developed damage in the form of surface wrinkling due presumably to plasticity by means of dislocation motion. Transmission electron microscopy studies are underway to confirm this hypothesis. The quasi *in-situ* test involving FE-SEM and automated EBSD revealed an evolution of grain structure and orientations, as shown in figure 4 for the first  $40 \text{ s}$  of the test. The four grayscale SEM images show localized surface wrinkling, while the color EBSD images show the growth of some grains at the expense of others. All images are taken from the same region, and the four color images represent the same sequence of accumulated time as that indicated for the



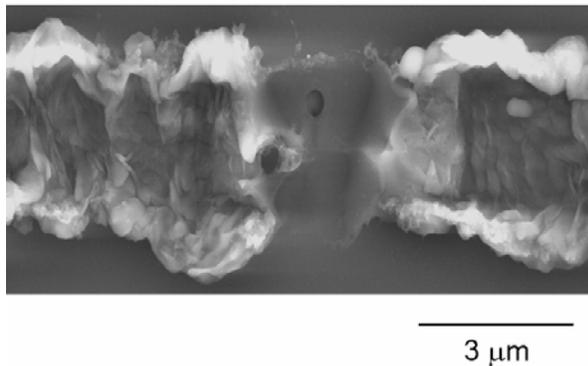
**FIGURE 3.** Current density versus lifetime for Al-1Si and Cu lines tested under AC conditions at  $100 \text{ Hz}$ . Vertical bars represent  $0.3 \text{ MA/cm}^2$  uncertainties in current density.



**FIGURE 4.** Quasi *in-situ* AC test results from Al-1Si line, showing development of surface damage, grain growth, and grain reorientation with increased cycling. Top sequence shows four grayscale SEM images from one region, bottom sequence shows corresponding color EBSD orientation maps from same region. Times represent total accumulated AC cycling times.

grayscale images. In the bottom four images, color changes with time represent changes in crystal orientation with cycling. We used Schmid factor contrast for this particular set of images, to represent the geometric relationship between the local crystal orientation matrix and the longitudinal direction of the line. The sequence of images shows that damage is detectable after only 10 s, or 1000 AC cycles; we note this corresponds to 2000 power or temperature cycles.

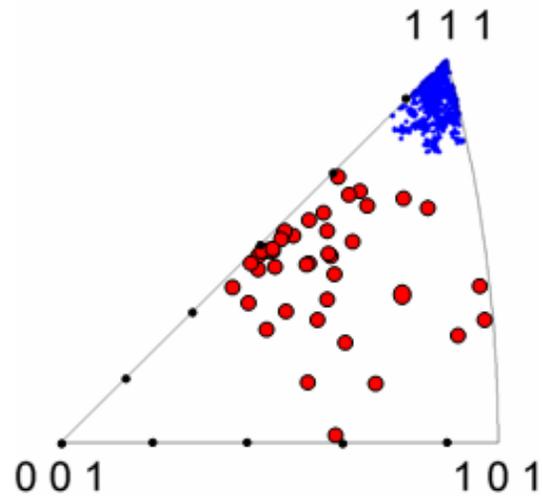
In all cases, failure of both Al-1Si and Cu lines took place in the form of open circuits. These failures occurred at locations of the line where severe changes in structure had taken place, as determined by SEM images of surface topography, and by EBSD determinations of grain structure and orientations. Figure 5 shows an example of an open circuit that developed at a region of severe deformation. Automated EBSD mapping revealed that surface normal orientations exhibited significant rotations in the heavily deformed regions, often in excess of 30°, as shown by the inverse pole figure in figure 6, which indicates the distribution of surface normal directions before and after AC cycling.



**FIGURE 5.** SEM image showing open circuit failure at region of severe deformation.

## DISCUSSION

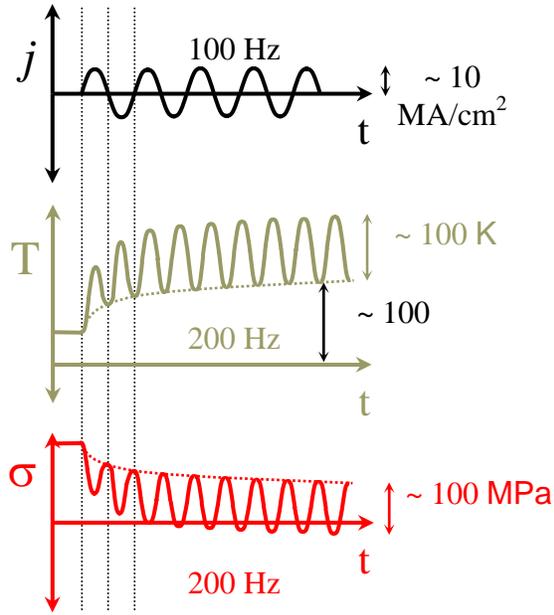
We provide first a general discussion of the applicability of electrical test methods to fatigue and other mechanical property measurements, followed by some comments on our results on thermomechanical fatigue in Al-1Si and Cu in the context of microstructural changes observed to occur during electric current-induced stressing.



**FIGURE 6.** Inverse pole figure (IPF) showing crystallographic orientations corresponding to surface normal directions. Blue points represent grain orientations prior to AC testing. Red points represent orientations of severely deformed regions after AC testing. Black dots along IPF edges represent 10° increments.

## Electrical Methods for Fatigue Testing and other Mechanical Properties

Thermomechanical fatigue is induced by low frequency, high current density AC stressing due to Joule heating. The power input into an interconnect during each power cycle is completely dissipated in the form of heat into the surrounding substrate and/or passivation (if present). This is because the thermal diffusivity of materials such as silicon or silicon dioxide is of the order of  $10^{-4}$  m<sup>2</sup>/s, allowing heat to flow over a distance of nearly 0.5 to 1 mm from the current-carrying interconnect into the surrounding materials during the period of one power cycle, or 0.005 s. Figure 7 shows schematically how the cyclic dissipation of heat leads to thermomechanical fatigue, where  $j$  = current density,  $T$  = temperature, and  $\sigma$  = stress. In terms of fatigue testing, the mechanical stress amplitude depends on the magnitude of the cyclic current density. The ratio of the minimum to the maximum mechanical stresses, often termed the fatigue R-value, can be varied by controlling the rms temperature of the test specimen through substrate heating or cooling. This would allow for tests encompassing tension-tension, compression-compression, or fully reversed tension-compression loading. Analyses of the temperature dependence of cyclic current flow and the frequency dependence of cyclic heat flow have been completed in reference [6].



**FIGURE 7.** Schematic showing relation between low frequency, high current density AC input into an interconnect and resulting temperature and mechanical stress behaviors as a function of time. Values for current density, temperature, and stress are order of magnitude examples.

We are in the process of exploring how electrical testing can be used to measure other mechanical properties of thin films and interconnects. One such possibility is to estimate the ultimate tensile strength by determining the fatigue ductility coefficient,  $\epsilon'_f$ , through the Coffin Manson relation:

$$\frac{\Delta\epsilon_p}{2} = \epsilon'_f (2N_f)^c \quad (1)$$

where  $\Delta\epsilon_p$  is plastic strain amplitude,  $N_f$  the number of cycles to failure, and  $c$  the fatigue ductility exponent. A series of tests involving large values of  $\Delta\epsilon_p$  and small  $N_f$  can provide a value for  $\epsilon'_f$ , which can then be used to estimate the ultimate tensile strength.

### Thermomechanical Fatigue of Cu and Al-1Si

Damage evolution as documented by SEM and EBSD exhibited heterogeneous behavior typical of plastic deformation in polycrystalline metals. In particular, surface topography was observed to occur in only selected regions of stressed lines, and only some grains showed growth and re-orientation. Localization of plasticity is even more typical of deformation that takes place during cyclic deformation

of metals. Repeated loading, especially to stresses near the macroscopic yield strength, provides dislocations with many opportunities to overcome localized slip barriers in the metal to create accumulated displacement, and to form lower energy configurations, such as dislocation walls, cells, or persistent slip bands (in the case of face-centered cubic metals), than those seen during monotonic loading. The detailed processes are somewhat different for thin film materials, but the general principles of plastic deformation still apply. Plasticity becomes especially pronounced in grains where a combination of the following factors can favor significant dislocation activity: (i) the resolved shear stress on preferred crystallographic slip systems exceeds the average such value for the entire polycrystalline aggregate; (ii) grains are sufficiently large to exhibit low yield strengths; and (iii) dislocations may be easily nucleated, based on the availability of likely sources such as grain boundaries with highly random structure.

We suggest that open circuit occurred after localized deformation caused a severe enough reduction in localized cross-sectional area of the line to drastically increase the localized current density to the point of causing melting.

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