Thermal fatigue testing of thin metal films

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An experimental method is described for performing thermal fatigue testing of thin films and lines on substrates. The method uses Joule heating from alternating currents to generate temperature, strain, and stress cycles in the metal structures. The apparatus has been installed in a scanning electron microscope and allows *in situ* observations of the fatigue damage evolution. First observations on Cu films reveal that fatigue damage forms in submicrometer thick films and is strongly affected by the film thickness and grain size. In addition, results from a special test structure confirm that the damage is caused by fatigue and not by electromigration. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1809260]

I. INTRODUCTION

Thermal fatigue is a threat in any composite system that experiences thermal cycles during use. Historically, thermal fatigue has been a major reliability threat in systems used in structural applications. More recently, concerns have been raised about thermal fatigue in much smaller structures.[1–4] For instance, extensive work has been performed on predicting thermal fatigue failure of the components of electronic packages with dimensions on the order of 10–100 μm.[2] Thermal fatigue is even a concern in metal structures with submicrometer dimensions, such as the lines found in microelectronic circuits and microelectromechanical systems.[1,4]

Fatigue damage and failure in bulk materials are based on the formation of stable dislocation structures with length scales on the order of a micrometer. Therefore, it is reasonable to question whether fatigue in submicrometer structures proceeds in the same fashion as in bulk materials, since dislocation nucleation and motion are constrained by small dimensions.[5–8] This question is even more relevant for thermal fatigue, where diffusion-controlled processes which are promoted by elevated temperatures may proceed differently in small scale structures containing a high density of interfaces. Several observations of fatigue in thin metal structures show that although some of the characteristic features of fatigue are still present, the samples show significantly different fatigue behavior from their bulk counterparts.[1,4,9–16] Both the fundamental issues and the potential threat to various applications provide strong reasons to study thermal fatigue in small scale structures.

This article describes a method and an apparatus for thermal fatigue testing of thin films on substrates and presents results of *in situ* scanning electron microscopy (SEM) observations of thermal fatigue damage in Cu films. The basic concept underlying the method is the use of controlled Joule heating, by means of alternating currents, to introduce temperature cycles in the films. The temperature cycles, in combination with the unavoidable mismatch in coefficients of thermal expansion, lead to cyclic straining of the metal films and eventually to damage formation.[1,4] The method is well suited for *in situ* adaptation and has been implemented in a scanning electron microscope, where the initial tests on Cu lines were performed. The majority of the article will address the experimental setup and the cyclic temperatures generated in the metal. Some first observations of fatigue damage in Cu lines will be presented and the role of the electrical currents in damage formation will be addressed. Then, advantages and disadvantages of the method in comparison to conventional fatigue experiments will be discussed. Finally, some of the implications for the reliability of interconnects in microelectronic devices will be mentioned.

II. TEMPERATURE IN A CURRENT-CARRYING METAL LINE

A current-carrying metal line experiences a temperature increase due to Joule heating. For a metal line on a substrate, such as illustrated in Fig. 1(a), most of the heat generated in the line is conducted away by the metal and the underlying substrate. The temperature of the line is determined by the line and substrate geometries, the thermal conductivities of the materials, and the presence of a heat sink or reservoir.

Despite the straightforward concepts behind heating in current-carrying lines, solutions to the temperature distributions are generally quite complicated. For example, no simple analytic expression is available for the geometry shown in Fig. 1(a), or even for the simpler two-dimensional case of an infinitely long line on a substrate. However, finite element analysis (FEA) is well suited to modeling such prob-

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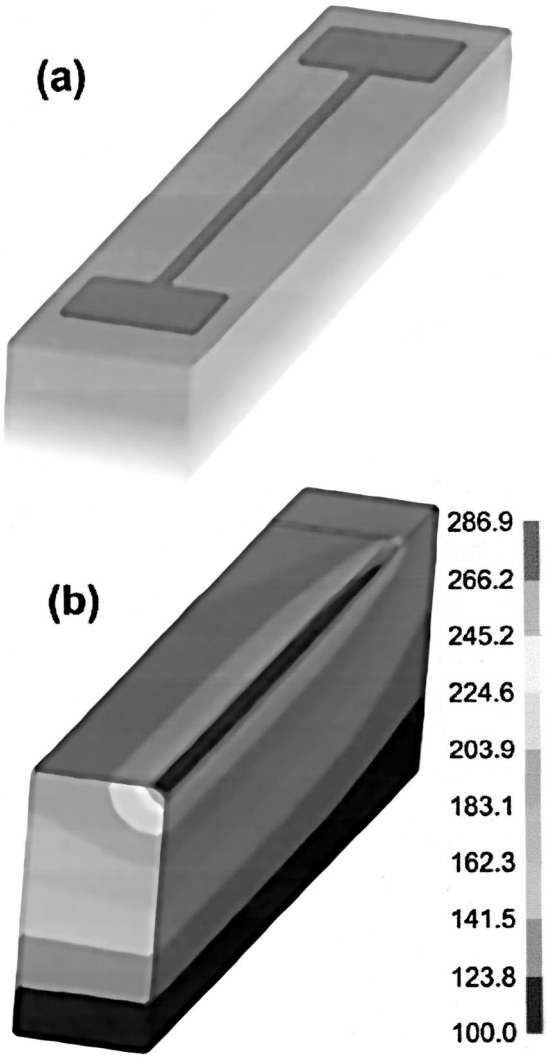


FIG. 1. (a) Schematic of line structure used for testing. The line is 800 μm long, 8 μm wide, and 0.3 μm thick. The region that is modeled by FEA is outlined with a dashed line. (b) FEA contour plot of temperatures (100 °C) due to Joule heating in the line.

lems. A steady state temperature distribution is shown in Fig. 1(b), which was calculated using temperature-independent thermal and electrical properties and applying a dc voltage of 8 V to an 800-μm-long Cu line directly on Si. The temperature of the lower side of the 100-μm-thick wafer was held at a constant temperature of 100 °C, providing a heat reservoir for the sample. Figure 1(b) shows that there is a temperature gradient across the Si which results in heating of the line. As expected, the steady state temperature difference between the line and the reservoir is found to be proportional to the power dissipated in the line and is determined by the thermal properties of the materials lying between the line and the reservoir.

When an alternating voltage rather than a constant voltage is used, the sample experiences temperature oscillations. The magnitude of these oscillations depends not only on the sample geometry and materials, but also on the frequency. For very low frequency signals in samples that are in good thermal contact with a heat reservoir, the sample remains in steady state during the power cycles and the temperature

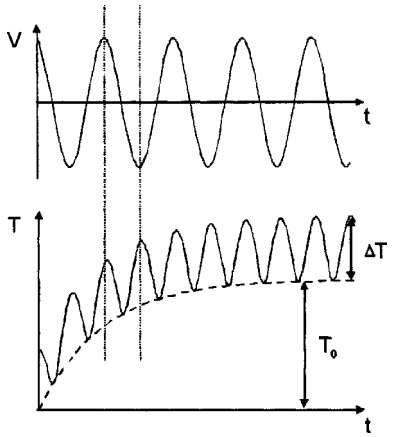


FIG. 2. Schematic illustration of voltage and temperature during ac testing, including the transient (dashed line) and periodic component. The temperature oscillations occur at twice the frequency of the voltage oscillations.

difference between the line and the reservoir remains proportional to the instantaneous power dissipated throughout such a cycle. For instance, if a sinusoidal voltage $V_0 \sin \omega t$ is applied to the line, the instantaneous dissipated power is $V_0^2 \sin^2 \omega t/R = V_0^2(1-\cos 2\,\omega t)/2R$, where R is the line resistance. Thus the temperature difference between the line and the reservoir will swing between zero and a maximum value proportional to V_0^2/R at *twice* the frequency of the electrical signal.

At higher frequencies, there is not enough time for steady state to be reached and the temperature difference is no longer proportional to the instantaneous power. For example, for frequencies higher than roughly 15 Hz, the thermal wavelength $(D/2\omega)^{1/2}$ of Si is of the order of or below a typical substrate thickness of 525 μm used in the microelectronics industry. D is the thermal diffusivity of the substrate. The temperature in the line will still have a periodic component at twice the frequency of the electrical signal, but it will be superimposed on a slower transient. The transient is caused by heating of the substrate and the underlying sample holder due to the time-averaged power. After a characteristic time, which depends on the thermal conductivity and thermal capacitance of the sample, the transient will have saturated, but steady, periodic temperature oscillations will continue to occur. This situation is illustrated schematically in Fig. 2, where the transient results in a temperature increase T_0 and the periodic component causes cycles with a total temperature range ΔT (two times the temperature amplitude).

An infinitely long and infinitely narrow line on a semi-infinite substrate can serve as a model to study the frequency behavior of the temperature oscillations. This problem has been solved analytically for the case of a periodically heated line source.[17,18] After the transient has saturated and caused a temperature increase of the line and its surrounding materials, the steady periodic temperature oscillations of range ΔT can be calculated. In the immediate vicinity of the line (at a distance from the line much smaller than the thermal wavelength $(D/2\omega)^{1/2}$), the solution for the temperature range ΔT can be approximated as

$$\Delta T = \frac{Q}{\pi \cdot k}(-\ln(2\omega)/2 + \text{const}), \quad (1)$$

where Q is the amplitude of the power per unit length in the line, $\omega/2\pi$ is the electrical signal frequency, and k is the thermal conductivity of the substrate. Thus, the amplitude of the periodic component of the temperature is expected to be proportional to the power and to fall off as the logarithm of the signal frequency. For very high frequencies, the amplitude of the periodic component becomes very small, because most of the power is dissipated in heating the thermal mass of the line and its immediate surroundings and less power remains for the flow which causes the temperature gradients.

III. EXPERIMENTAL DETAILS

A. General setup

Copper lines fabricated on silicon chips, such as the one shown in Fig. 1, were used to test and optimize the thermal fatigue setup. The chips were mounted on a temperature-controlled heater block in the chamber of a SEM and electrical connections were made to the contact pads of the Cu line structure using a motorized needle probe station. Temperature cycles were generated by applying a sinusoidally alternating electrical voltage to the lines. This method has been used previously,[1,4] except here the temperature in the Cu line was measured during the experiment. The temperature ranges of the cycles were determined from four point resistance measurements and, due to the mismatch in thermal expansion coefficients between the metal and the substrate, resulted in strain and stress cycles, which caused thermal fatigue in the lines. The evolution of the fatigue damage during testing was monitored using SEM imaging. In order to obtain good quality images, the alternating voltage was turned off while the sample was imaged to avoid deflection of electrons by the magnetic fields set up by the alternating current in the Cu lines.

Voltage control rather than current control was used for the experiments to minimize "run away" local heating in damaged regions due to resistance increases. Performing the experiments with a fixed voltage amplitude also allowed better control of the sample temperature, since as the sample temperature increased at the beginning of each experiment, the resistance also increased and the average power ($\sim V_0^2/R$) decreased. However, voltage control made the use of established methods for temperature measurement (e.g., the 3ω method[18]) very complicated.

The sinusoidal voltage signal was applied to the test structures using a signal generator and an amplifier as illustrated schematically in Fig. 3. A signal frequency of 100 Hz was used in the tests presented here, but could be varied from dc to roughly 20 kHz. The voltage amplitude was adjusted to reach the desired temperature range ΔT in the line. For the geometries and structures used here, the voltage amplitudes were between 3 and 8 V which resulted in current amplitudes between roughly 0.6 and 1.0 A (14–24 MA/cm^2), and maximum powers between 2 and 8 W. The dc component was minimized and typically below 5 mA.

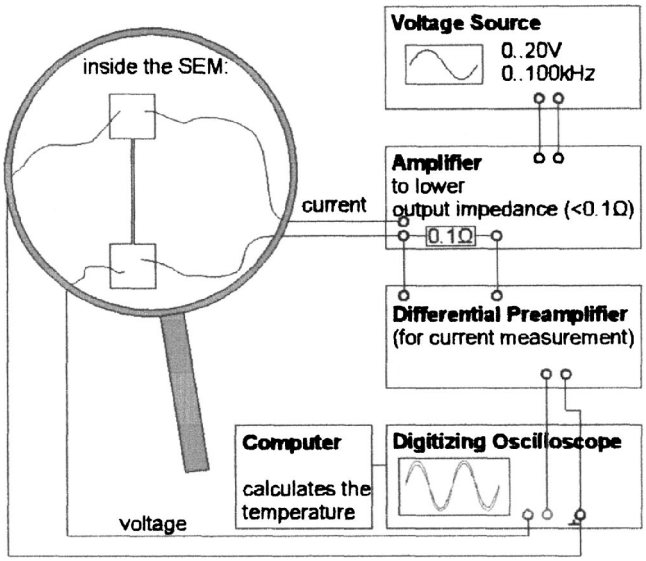


FIG. 3. Schematic illustration of the testing setup.

The time-resolved voltage $V(t)$ and the resultant current $I(t)$ in the test structure were monitored with a digital oscilloscope. Due to the temperature variation during the cycles, the current signal is not sinusoidal as can be seen by comparing the voltage and current in Fig. 4(a). The noise in these time-resolved measurements was reduced by averaging over several cycles and the time-resolved resistance was calculated from the voltage and current signals. A typical resistance trace is shown in Fig. 4(b) for a signal frequency of 100 Hz. As expected, the resistance varied periodically at twice the frequency of the applied voltage due to the temperature variations created by Joule heating. The scatter in the smallest values of resistance comes from the fact that the

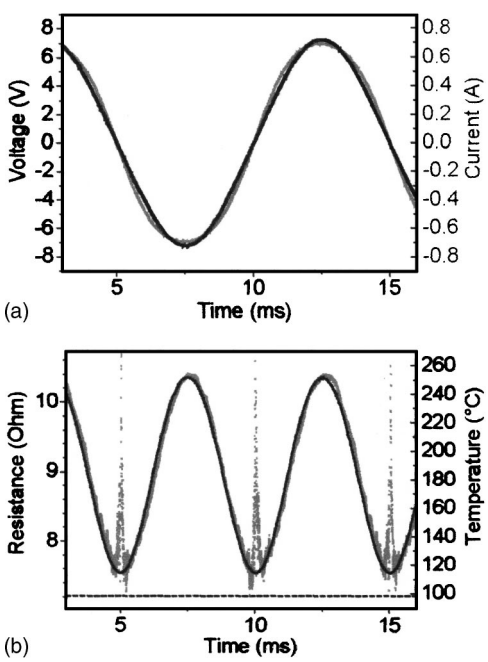


FIG. 4. (a) Voltage (black) and current (gray) as a function of time. (b) Resistance (data points) and temperature determined using an instantaneous power fit (line). Dashed line corresponds to the temperature measured by the thermocouple cemented to the edge of the Si chip.

voltage and current both pass through zero at this point in the cycle. The temperature of the Si chip was measured using a fine gauge wire thermocouple cemented to a corner of the chip. This thermocouple was used to measure the transient temperature increase (illustrated in Fig. 2) at the beginning of each test due to overall heating of the sample and the underlying sample holder. The thermocouple temperature rose for a period of roughly 1–2 h and then saturated at a value of T_0 between 70 and 110 °C depending on the voltage signal amplitude. To bring the chip more quickly to this temperature, a temperature-controlled heater installed in the block underneath the sample was used to heat up the sample and its surroundings before the tests were started, and then was turned off during the test. With this method, a steady value of T_0 could be reached within 15 min of starting the test. This heater was also used in order to have independent control of the average sample temperature during a test. This allowed additional heating of the sample up to a maximum temperature of 400 °C. Limited cooling of the sample could also be achieved using a Peltier element cemented between the Si chip and the heater block, which provided up to roughly 40 °C of cooling during a typical experiment.

B. Sample description

The Cu line structures used for the tests were prepared using electron beam lithography, sputter deposition, and a lift-off step. Small pieces (1 cm by 1 cm) of oxidized Si, 525 μm thick with 50 nm of SiO_2 on the top and bottom surfaces, were coated on one side with photoresist and exposed in a SEM. After development, 5 nm of Ta and 100 or 300 nm of Cu were deposited without a vacuum break onto the substrates using magnetron sputtering. Lines 8–15 μm wide, 100 or 300 nm thick, and roughly 800 μm long were formed by dissolving the photoresist. The 5 nm Ta layer was necessary for adhesion of the Cu to the substrate during the lift-off step. After fabrication, the samples were annealed in a vacuum oven at 400 °C for 15 h in order to allow for grain growth and to stabilize the microstructure. Focused ion beam microscopy revealed a heavily twinned columnar grain structure with grain sizes of roughly 0.3 and 1.5 μm in the annealed 100- and 300-nm-thick films, respectively. θ-2θ x-ray diffraction measurements showed that the films had a predominately $\langle 111 \rangle$ out-of-plane texture with a small $\langle 100 \rangle$ component.

C. Temperature measurements

The temperature dependence of the resistivity of the Cu line samples was determined by heating the sample in the vacuum chamber of the SEM using the heater block. The line resistance and temperature of a thermocouple cemented to the Si chip were recorded during cooling back down to room temperature. The thermocouple gives an accurate measure of the line temperature during slow cooling since loss of heat by radiation is negligible.[18] It was found that the resistance increased linearly with temperature and that the temperature coefficient, $(dR/dT)/R_0 = 3.6 \times 10^{-3}/\mathrm{K}$ agreed well with values in the literature for bulk Cu. There was some variation in the absolute value of the room temperature resistance from structure to structure, presumably due to variations in line geometry. However, the temperature coefficient of the resistivity remained constant to within 1% for all of the structures measured.

The time-resolved resistance can be used to determine the temperature in the Cu line from the measured temperature dependence of the resistivity. However, in practice this process is complicated by two effects. First, there will be temperature nonuniformities along the line. As shown in the FEA calculated temperature distribution in Fig. 1(b), the temperatures at the ends of the line are lower than those in the middle of the line due to the flow of heat into the contact pads. The line temperature increases rapidly with distance from the pad, reaching 90% of the peak temperature (which occurs at the middle of the line) at a distance of 25 μm from the pad and reaching 99% at a distance of 140 μm from the pad. Using the FEA predictions of the temperature distribution along the line, a correction factor (1.031) was obtained to account for the smaller resistance contribution from the cool ends of the Cu line and to accurately predict the temperature in the central uniformly heated region of the 800-μm-long lines studied here. FEA was further used to estimate the effect of resistance inhomogeneities in the line. These are expected after severe damage has formed, such as a crack that partially spans the line. The calculations show that, for example, a temperature increase of only a few degrees is caused by a crack that spans one third of the linewidth. Thus, the heat is effectively distributed by the Cu line and the Si substrate and local heating due to defects can be neglected up until shortly before failure.

The FEA calculations that have been used for comparison with the experiments are somewhat simplified relative to the actual conditions. Due to periodic boundary conditions, the FEA model represents an array of periodically spaced current carrying lines rather than the single, isolated line used in the experiments. Also, the Si wafer in the model is thinner that that used in the experiments. And, the underlying SiO_2 layers, both those between the metal and the Si and between the Si and the reservoir, have been neglected in the calculation. Similarly, the small effect of interface resistances[19] has been neglected. Also, deviations from the bulk thermal constants due to the small length scales have been ignored.[19] The use of these simplifications in the FEA model mean that the absolute temperature predictions will not be accurate, but the basic trends are believed to be reliable.

The second effect that complicates the determination of the temperature from the time-resolved resistance is the noise in the data when the current and voltage signals pass through zero. This makes it difficult to accurately determine the minimum temperature T_0. One method to compensate for this effect is to assume that the temperature in the line is proportional to the instantaneous dissipated power, $V(t)I(t)$. Such an assumption ignores the effects of temperature dependent material properties, heat losses by radiation, and phase shifts between the temperature and the power signals. A fit to the resistance data using this assumption is included in Fig. 4(b) and fits the data very well. Also included in the plot is the temperature measured by a thermocouple cemented to a corner of the Si chip. For frequencies as low as 100 Hz, the

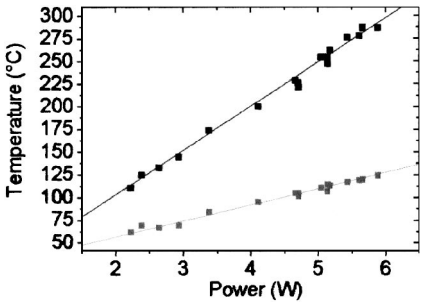


FIG. 5. Minimum and maximum temperature in eight different test structures plotted against the applied peak power. The scatter in the temperature data is mainly due to scatter in the minimum temperature which results from not allowing the initial transient to reach saturation.

thermocouple temperature lies somewhat below the minimum temperature in the line.

Plots of the minimum temperature T_0 and the maximum temperature $T_0+\Delta T$ are shown as a function of the applied peak power in Fig. 5. Both temperatures could be determined with a precision of roughly ±3 °C using the described method. The fact that both T_0 and ΔT scale linearly with the power supports the idea that radiative heat losses from the sample are negligible in comparison with the heat conducted away through the Si[18] and that the temperature dependence of the material properties (other than the resistance) can be ignored. The relatively small scatter in the data means that the desired temperature range can be accurately selected by choosing the appropriate peak power.

A plot of the temperature range ΔT as a function of the signal frequency for constant applied voltage amplitude is shown in Fig. 6. A constant maximum power of 4.5 W was applied and the minimum and maximum temperature in the line were recorded at different frequencies. The temperature of the thermocouple attached to the corner of the Si stayed nearly constant between 102 and 105 °C for all of the frequencies. As expected from Eq. (1), ΔT falls off with increasing frequency, so that larger and larger powers are needed to reach a desired temperature range. This increases the average temperature T_0 and eventually makes the tests impractical. With a linear fit to the data at lower frequencies using Eq. (1), a value of the thermal conductivity of 82 W/mK was obtained. This agrees well with literature data for Si at 500 K. However, above 6 kHz, ΔT falls off more rapidly with frequency. This can be understood by considering the sample geometry in conjunction with the thermal wavelength $(D/2\omega)^{1/2}$. At 100 Hz, the thermal wavelength is on the order of 200 μm, but for a frequency of 6 kHz, the thermal wavelength is only two or three times larger than the linewidth. The observed behavior at high frequencies can presumably be understood as the transition from a regime where the line acts as a line heat source to a regime where the line acts as a planar heat source. For a planar heat source, ΔT is proportional to the inverse of the square root of the frequency[20,21] and falls off more quickly with frequency than for a line source [Eq. (1)], explaining the behavior shown in Fig. 6.

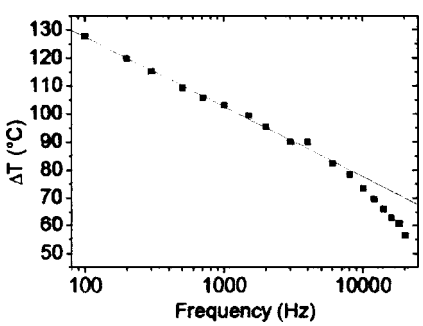


FIG. 6. Temperature range ΔT as a function of applied frequency for a constant power amplitude. The solid line is a fit to the data using the solution for a line heat source at the surface of a semi-infinite solid [Eq. (1)].

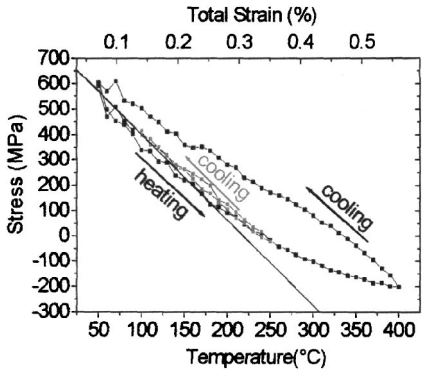


FIG. 7. Stress during temperature cycling (black points) in a 300-nm-thick Cu film. The total strain change imposed on the Cu film by the temperature change is shown on the top axis. The gray points show a thermal cycle over a typical temperature range of a fatigue test. The thermal-elastic slope for a ⟨111⟩ out-of-plane oriented film is shown as a solid line. Arrows indicate the direction of heating and cooling.

D. Thermal stresses

Due to the difference $\Delta\alpha$ between the thermal expansion coefficients of Cu $(17\times10^{-6}/°C)$ and Si $(3\times10^{-6}/°C)$, the temperature variations cause strain cycles in the line. Assuming $\Delta\alpha$ is temperature independent, the total biaxial strain amplitude due to the temperature cycles is given by $\Delta\varepsilon=\Delta\alpha\Delta T$. In writing this equation, several approximations have been made. Strain relaxation at the line edges has been ignored, which is reasonable in lines which are much wider than they are thick. In addition, the fact that the Si underneath the Cu line is somewhat cooler than the line itself [Fig. 1(b)] has been ignored since it has only a small effect on the strain amplitude in the line.

The imposed strains result in both elastic and plastic responses in the Cu lines. These can be estimated from the measured stress in a continuous film prepared by the same deposition process as the line structures. Figure 7 shows wafer curvature measurements of the stress from such a film during thermal cycling in a controlled atmosphere oven.[7] On heating from room temperature, the initial biaxial tensile stress in the film decreases and becomes compressive, roughly following the thermal-elastic slope for a ⟨111⟩ out-of-plane oriented Cu polycrystal (solid line in Fig. 7). Contributions from the 5-nm-thick Ta film to the stress curves were assumed to be negligible. At around 200 °C, the stress deviates from the elastic slope, indicating the onset of macroscopic plasticity. Plasticity continues to determine the

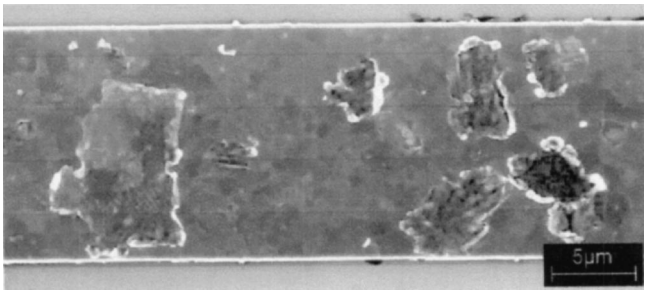


FIG. 8. Damaged patches in a 300-nm-thick Cu line after testing at $\Delta T \sim 170\ ^\circ\mathrm{C}$ (imposed total strain range of 0.24%) for 3.3×10^5 cycles.

stress behavior up to the maximum temperature. On cooling, the stress first increases elastically, and then begins to deform plastically below 250 °C. Based on the cycles shown in Fig. 7, a thermal cycle between 50 and 400 °C imposes a total strain range of 0.49% on the sample and results in a total stress amplitude of 800 MPa with considerable plasticity. A cycle between 100 and 250 °C imposes a total strain range of 0.21% on the sample and gives a completely tensile cycle with a total amplitude of 400 MPa with very little macroscopic plasticity.

The difference between the stress state in the film, determined using wafer curvature measurements, and in the finite width line used in the thermal fatigue tests can be ignored to first order since the substrate is relatively stiff and the linewidth is much greater than the line thickness. However, a number of important differences are expected due to issues such as cycle frequency (1 h was typically required for a single wafer curvature cycle) and number of cycles. Most importantly, the stress–strain curves are expected to change and evolve during fatigue testing due to fatigue hardening or softening of the metal.[22] Thus, the wafer curvature measurements provide only an estimate of the stress in the samples during thermal fatigue testing.

IV. FATIGUE DAMAGE IN COPPER LINES

Fatigue tests were performed for several different temperature ranges ΔT from 120 to 190 °C and for up to 2×10^8 cycles. The minimum temperature T_0 was between 70 and 130 °C during all tests. The voltage signal frequency was 100 Hz. In all cases except the smallest temperature ranges, damaged patches were observed to form during testing along the length of the Cu line. In general, the patches were evenly distributed along the length of the line except in regions close to the contact pads where no patches were observed, presumably because the temperature amplitudes are smaller in these regions. Figure 8 shows several damaged patches in a region of a 300-nm-thick line after 3.3×10^5 cycles at a temperature range of 170 °C (imposed total strain range of 0.24%). In the damaged region at left, parallel surface wrinkles can be seen. These surface wrinkles are similar to the parallel extrusions and intrusions observed at the surface of mechanically fatigued bulk metals.[22] A cross section of one of the wrinkled regions made using a focused ion beam microscope revealed that the intrusions extended almost to the substrate.

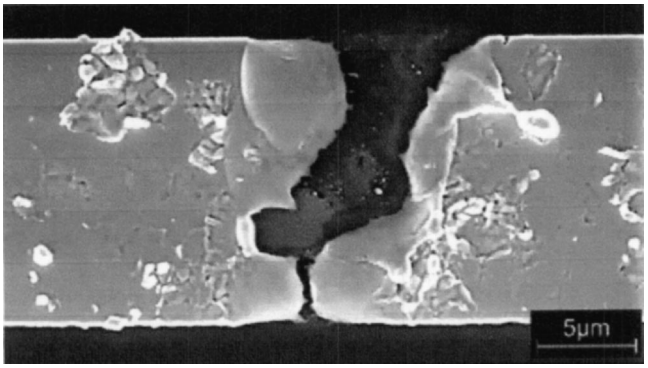
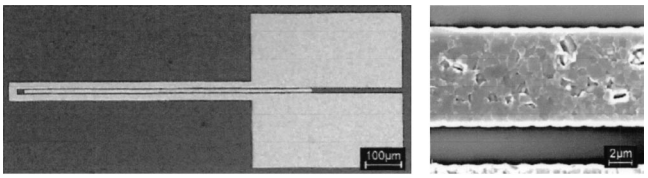


FIG. 9. Failure site in a 300-nm-thick Cu line after testing at $\Delta T \sim 180\ ^\circ\mathrm{C}$ (imposed total strain range of 0.25%) for 2.0×10^5 cycles.

As the number of cycles was increased, the damage in the 300-nm-thick Cu lines became more severe and eventually the lines failed by an electrical open. A typical failure site is shown in Fig. 9. The edges next to the failure site look as though they have melted during the failure process. This presumably occurs because a decrease in the line cross section, possibly near an intrusion, results in current crowding and local heating which eventually causes local melting and failure. A series of experiments to determine the number of cycles to failure revealed a strong dependence on the temperature amplitude. For ΔT of 120 °C (imposed total strain range of 0.17%), no failure could be found even after 5×10^7 cycles. For larger ΔT, failure happened more quickly and at the highest ΔT of 190 °C (imposed total strain range of 0.27%) failure occurred within as few as 1×10^5 cycles. The fact that the number of cycles to failure decreases with increasing ΔT, or strain amplitude, is consistent with general fatigue behavior.

Fatigue damage was also observed in the 100-nm-thick films. In these films, the damage appeared as thinned grains, hillocks, and grain boundary grooves all along the length of the line. Wrinkled damaged patches (such as shown in Fig. 9) were occasionally observed, but only in the largest grains of the 100 nm films. In addition, the number of cycles to failure of the 100-nm-thick films was up to two orders of magnitude higher than that of the 300 nm films for a given temperature amplitude. This increase in the number of cycles to failure with decreasing film thickness supports previous observations on mechanically fatigued Cu films.[14] The change in the damage morphology reveals that with decreasing grain size and film thickness, fatigue appears to be more and more controlled by diffusive mechanisms and interface properties rather than by dislocation glide.

Although the alternating current densities used here are large in comparison with those used in dc electromigration experiments, the damage observed here does not look like typical electromigration damage. Typical electromigration damage usually appears as depletion at one end of the metal line and hillock formation at the other[23] and is caused by a current-induced atom motion in the direction of the electron flow. Early stage electromigration damage can be "healed" by reversing the current, which explains why it is not observed under high frequency ac tests.[24] Nonetheless, to rule out contributions from electromigration-induced atom trans-



(a) (b)

FIG. 10. (a) Schematic illustration of structure used to test for electromigration-induced damage. The inner line is electrically isolated from the outer line and carries no current. (b) Damage in the middle line has formed without a current.

port in the experiments made here, tests were performed with a special test structure in which temperature oscillations could be introduced without current. The test structure is illustrated in Fig. 10(a). A sinusoidal voltage signal was applied to the outer, wider line using the contact pads. The middle, narrower line experienced temperature oscillations due to the current in the neighboring wider lines, although it carried no current. The magnitude of the temperature oscillations in the middle line was estimated from two-dimensional FEA calculations as being roughly 0.93 of the temperature oscillations in the outer lines. Following $\sim 10^5$ cycles at a temperature range of $\sim 250\ ^\circ\mathrm{C}$ in the outer lines, damaged patches were observed to have formed in both the outer and middle lines. An image of the damage formed in the middle line is shown in Fig. 10(b). The damage looks different from that in Fig. 8 due to the finer grain size in these structures. Nonetheless, it provides unequivocal evidence that the damage observed in the experiments presented here is predominately due to thermal fatigue and not to electromigration-induced atom transport.

V. DISCUSSION

Compared to conventional fatigue experiments, this method has several advantages. The most obvious advantage is the ease of use. In typical fatigue experiments, tensile/compressive tests are performed by precise mechanical equipment. Therefore the frequency of the experiments is limited and experiments are difficult to perform when the size of the specimens is in the micrometer range. In contrast, ac induced fatigue testing does not rely on any mechanical parts or specimen clamping and therefore very small samples can be examined. Instead of complicated equipment for applying and measuring force and displacement, only electrical contacts are needed to supply the power and apply the strains. This offers the possibility of performing the experiments *in situ*, to investigate the damage locally during testing as shown here in a SEM. The frequency of the tests is only limited by the sample dimensions and thermal diffusivities, therefore experiments on a wide range of frequencies from 1 to 10^4 Hz (and presumably higher depending on materials) can be run. Further application of this method, for example, to *in situ* transmission electron microscopy is certainly possible although the appropriate electrical power and frequencies will need to be carefully considered in a geometry where thermal contact to the sample is difficult.

One major limitation of this method is that the strain and the temperature cannot be varied independently. This fact also means that the maximum strain range is limited by the difference between the thermal expansion coefficients of the metal and the substrate and by the applied temperature range. A second major limitation is that the stresses cannot be measured during testing. This is an important issue, because most metals undergo cyclic hardening or softening during fatigue tests. Thus, when experiments are performed under strain control, the stresses during testing may deviate from the stresses measured at the beginning of the tests, limiting the utility of wafer-curvature-determined stress–strain curves.

Due to effects of high current densities and temperatures used in these experiments, electromigration, thermomigration and other diffusive processes can contribute to damage processes. However, the damage observed here in Cu films is to first order generated by cyclic loading and is not caused by electromigration. There may still be small effects from electromigration, and once damage has formed and thermal gradients are present, thermomigration issues may also contribute.[25] Since these effects are all strongly temperature dependent, they can be minimized by keeping the average temperature in the sample sufficiently low.

Preliminary observations of fatigue damage and failure have been obtained using this method from 100- and 300-nm-thick Cu lines. The results show that despite the small dimensions, fatigue damage does form in thin films, although it depends on the film thickness and grain size. In the 300-nm-thick Cu films, the parallel surface wrinkles reveal that damage formation is controlled by repetitive dislocation glide, just as it is in bulk metal samples. In the 100-nm-thick Cu films, dislocation motion appears to be hindered by the small volumes and fatigue damage formation is controlled by diffusion along boundaries and surfaces.

The prevalence of fatigue damage and failure, even in small samples, suggests that thermal fatigue may be a reliability threat to the interconnects of microelectronic devices. The interconnects in typical microelectronic devices experience temperature variations due to the power dissipated in the interconnects and transistors. Although the clock frequency in modern devices is around a GHz—which is too high to produce a significant temperature amplitude—lower frequency temperature variations are still expected. The exact temperature-frequency spectrum at a given location in a device will depend on the chip architecture, electrical layout, and the particularly application being run. The results presented here show that damage occurs for temperature ranges as small as 150 °C. This is not much greater than the 100 °C temperature increase that is allowed in high performance devices during use. Current roadmaps for microelectronic devices include introducing interlevel dielectric materials with low thermal conductivities and low elastic modulii. These materials may worsen the threat to interconnect reliability from thermal fatigue by causing larger temperature cycles and reducing the mechanical constraint on the metal interconnects. Future results from studies of this kind may help to further reveal the effect of length scale on mechanical properties and to help better assess the reliability threat from thermal fatigue in the small metal structures used in many applications.

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