Stable 1 volt programmable voltage standard

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Several fully functional programmable voltage standard chips, each having a total of 32 768 Nb–PdAu–Nb Josephson junctions, have been fabricated and tested. The chips are based on a new design that provides fast programmability (1 μs) between voltages and stable voltage operation from -1 to $+1$ V. A comparison of the new standard with a conventional Josephson voltage standard is in agreement to 0.5 ± 1.1 parts in 10^9. We demonstrate the utility of this standard by measuring the linearity of a digital voltmeter. © *1997 American Institute of Physics.* [S0003-6951(97)04739-6]

In this letter, we demonstrate a new dc voltage standard that is both quickly programmable (1 μs) and inherently stable over the range from -1 to $+1$ V. The circuit uses superconductor-normal-superconductor (SNS) Josephson junctions and relies on the well known frequency to voltage conversion property that is the basis for the Josephson representation of the SI volt.[1] By combining SNS junction technology with appropriate microwave and dc bias circuits, we achieve microsecond programmability between steps and inherently stable voltage operation, features that are not possible with conventional Josephson voltage standards.

When an ac current of frequency f is applied to a Josephson junction, the current–voltage ($I-V$) curve of the junction exhibits equally spaced constant voltage steps at voltages $V=nf/K_J$, where the step number n is an integer. $K_J\equiv 483\,597.9$ GHz/V is the Josephson constant and is related to the unit flux quantum $h/2e\approx 1/K_J$. Conventional dc Josephson voltage standards use a single series array of about 20 000 junctions. The junction parameters are chosen to yield a hysteretic $I-V$ curve in which all of the constant voltage steps span the same current range. Superconductor-insulator-superconductor (SIS) junctions with very low critical current density, about 20 A/cm^2, are used to generate these hysteretic $I-V$ curves. Any one of about 200 000 steps of the SIS array can be selected by adjusting a single low-impedance bias source. Unfortunately, the selection process is slow and, since the steps are metastable, noise can easily induce transitions between steps. Although perfectly adequate for dc reference calibrations, these qualities are undesirable in applications that require perfect stability and/or fast programmability.

The concept for the fast programmable standard was previously proposed and demonstrated by Hamilton *et al.* as a D/A converter having a series array of resistively shunted SIS junctions with nonhysteretic $I-V$ curves.[2] The microwave power is adjusted to simultaneously maximize the current amplitudes of the $n=0$ and ±1 steps. By using junctions with nonhysteretic $I-V$ curves, the steps are no longer metastable and can be uniquely selected by an appropriate choice of dc current bias. The array is segmented into a binary sequence of N smaller arrays. Each mth array of 2^m junctions, where $m=0,1,...,N$ is capable of producing constant voltages at 0 and $\pm 2^m f/K_J$. The voltage across all segments adds in series, so that any output voltage between $-2^{N+1}f/K_J$ and $+2^{N+1}f/K_J$ in steps of f/K_J can be selected by choosing appropriate bias currents for the array segments. We hoped that this circuit could be used to digitally synthesize accurate ac waveforms, but switching transients associated with the dc bias currents resulted in an unacceptable uncertainty in the generated waveform.[3] Since there is now an improved method for generating fast, accurate ac waveforms based on pulse-driven circuits,[4] we anticipate that the binary array design discussed here will be used primarily for rapidly programmable dc voltages.

SNS junctions are preferred over resistively shunted SIS junctions for the following reasons:[3,5] (1) Their higher critical currents ($I_c>1$ mA) provide greater output current and greater stability against thermal and electrical noise. (2) Their low internal resistance R of the normal metal barrier provides the desired nonhysteretic $I-V$ curve. (3) Their lower characteristic voltage I_cR of 10–40 μV leads to convenient and less expensive operating frequencies $f=I_cRK_J$ of 5–20 GHz. SNS junctions have been investigated for programmable voltage standards circuits using both low-T_c[5–7] and high-T_c superconductors.[8,9]

Figure 1(a) is a schematic of the SNS 1 V programmable voltage standard chip and Fig. 1(b) shows the physical layout of the chip. The 16 GHz drive power is transmitted into the Dewar on a 50 Ω semirigid coaxial cable. At the end of the cable, it is launched into a coplanar waveguide (cpw) network that is etched onto a 2×8 cm BeCu clad FR-4 printed circuit board. Three tees and six tapers divide the signal into four identical 50 Ω feeds. The ends of the BeCu coplanar strips form spring fingers that contact matching pads on the left side of the 1 cm$\times$1 cm chip. At each feed on the chip, there is a 10 pF dc blocking capacitor and a 50–25 Ω two-stage quarter-wave transformer. A splitter further divides each signal so that all together there are eight 50 Ω feeds into eight array segments of 4096 junctions each. After each array, the cpw transmission line is terminated by a 50 Ω resistor and 10 pF capacitor to ground. The 32 768 junctions are divided into 13 segments with 14 dc bias taps between them as shown in Fig. 1(a). The number of junctions in each of the 13 segments is: 128, 128, 256, 512, 1024, 2048, and 7 adja-

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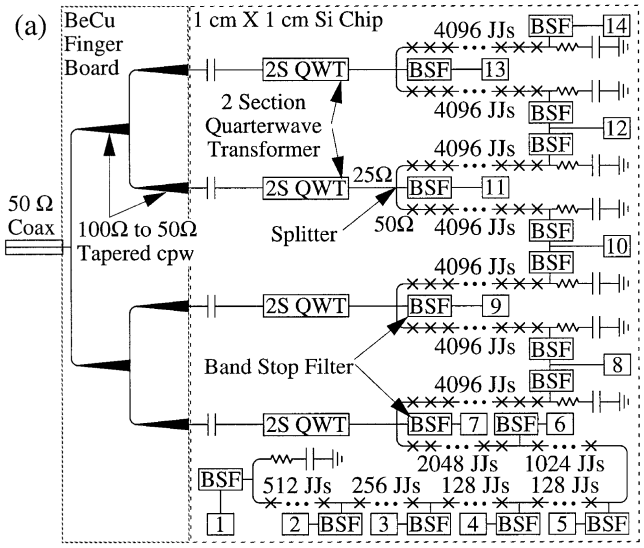

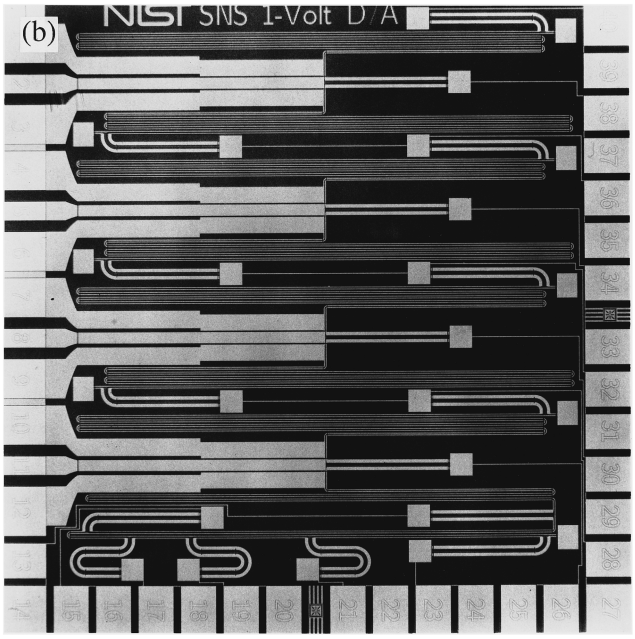

FIG. 1. (a) Programmable voltage standard schematic. (b) Photograph of 1 cm×1 cm chip showing physical layout.

cent segments each having 4096 junctions. Power uniformity requires that the taps on the array do not create reflections that would lead to standing waves. Each tap therefore includes a band-stop filter at the 16 GHz design frequency consisting of a quarter-wave section of 85 Ω coplanar line terminated by a 10 pF capacitor. The size of the band-stop filters prevents continuing the division all the way down to a single junction. A larger chip or more compact design would eliminate this limitation. The dc bias currents are applied through BeCu fingers to pads along the right and bottom sides of the chip. Further circuit design details and discussion are presented elsewhere.[6,7]

The conductors that define the SNS junctions are Nb–PdAu–Nb.[5] The junction critical current density is typically greater than 200 000 A/cm^2. The diameter of the junctions is 2 μm and the minimum circuit feature size is the 1 μm diam of the contact via above each junction. Nb wiring connects adjacent junctions through these vias. A critical

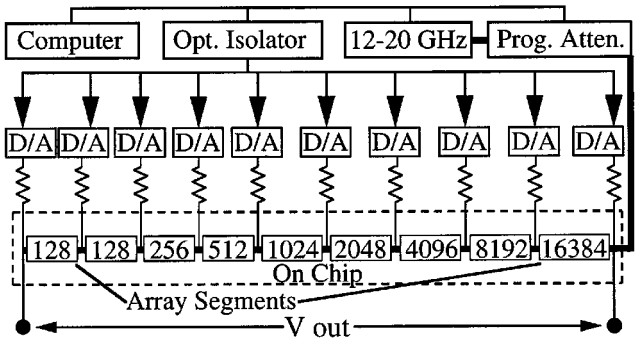

FIG. 2. The dc and microwave bias schematic.

technical goal of this work was the achievement of nonzero yield for this complex, large scale, superconducting integrated circuit. In order to achieve fully functional circuits, improvements were made in three areas: (1) the critical current of the Nb to Nb via contacts was increased to 30 mA (3 MA/cm^2), (2) the critical current of 6-μm-wide Nb wiring edge crossings was increased to 100 mA, and (3) alignment between the 32 768 vias and junctions was improved to ± 0.2 μm. Details of the fabrication process are described elsewhere.[6] Of the 12 chips on this 7.6 cm (3 in) wafer, 4 were 100% functional.

A schematic of the dc and microwave bias circuit is shown in Fig. 2. For chips with sufficient junction and power uniformity, 6 of the 4096 junction segments are combined so that the binary sequence of segments continues to 8192 and 16 384 junctions as shown. This arrangement requires fewer bias leads at the expense of circuit yield or operating range. The output voltage is adjusted from -1.08 to $+1.08$ V in steps of $128f/K_J = 4.2$ mV by applying the appropriate dc bias currents. The bias current in each segment is set by D/A converters at each end that push or pull current through the bias resistors. The D/A converters are controlled by a computer that calculates the currents and voltages required at each node of the array. The optical isolator allows the dc bias electronics to float so that either end of the array can be grounded.

The large critical currents (>1 mA) that allow minimal low pass filtering on the bias leads so that the switching time between voltages is less than 1 μs. A programmable signal generator and attenuator are computer controlled through IEEE bus ports. Computer control of the dc current, microwave power, and frequency is used for programming the output voltage and optimizing the bias conditions. Although the chip design frequency is 16 GHz, it operates from 12 to 20 GHz with some decrease in dc bias range and output current. Fine tuning of the output voltage is achieved by adjusting the microwave frequency. Subnanovolt resolution at 1 V is achieved by using a signal generator with 1 Hz resolution.

Both junction and microwave power uniformity are essential for successful operation. Since it is impractical to independently bias each junction, it is difficult to quantify uniformity for arrays of SNS junctions. The junction with the smallest critical current in each segment generally determines the operating range of that segment. For chips designed for 10 mA critical currents, the smallest critical cur-

rent for each segment typically varies $\pm 5\%$ (max. to min.) across the chip. When microwaves are applied, we can qualitatively determine the combined junction and power uniformity by comparing the bias current range, or step height, of the three steps for each segment.[6] For typical functional chips with uniform critical currents, the average $n=1$ step is centered at 14 mA with a variation of $\pm 5\%$ across the chip. Typical step heights are 3–5 mA for the $n=1$ steps and 7–9 mA for the $n=0$ steps. The $n=-1$ steps behave similarly to the $+1$ step. Power or junction nonuniformity in one array segment sometimes limits the applied microwave power such that the 0 and 1 step heights can not be equalized.

The chip used to perform the experiments described below was fabricated near the edge of the 76.2 mm diam (3 in) wafer, and consequently has a wider critical current distribution of 13.4 mA$\pm$10%. The step heights are 4 mA$\pm$30% for the $n=1$ step and 9 mA$\pm$20% for the $n=0$ step. The $n=1$ step centers range from 13 to 16 mA. This chip has wide operating margins with the smallest step height measuring 2.8 mA.

A comparison was performed between the voltage produced by one of the new SNS programmable voltage standards and a conventional SIS voltage standard. Each standard was operated in a separate Dewar. The SNS array was set to a fixed stable voltage of 1.000 000 0 V and connected in series opposition with a SIS array that was set to within a few millivolts of 1 V. To compensate for the circuit thermal emfs and null detector offset voltages, measurements were made with both voltage polarities. Wiring connections remained fixed during all measurements. A $+--+$ measurement sequence was used to eliminate offsets and linear drifts. The nanovoltmeter used to measure the difference voltage was placed with one of its input terminals connected to the grounded end of the SNS array so that its common mode response did not introduce a significant offset when the voltage polarity was reversed. Because of inadequate temperature control in the laboratory, the gain and linearity of the nanovoltmeter were calibrated several times over the period of the measurements by setting the SNS array to 0 V and allowing the SIS array to spontaneously switch to a number of voltages covering the range ± 10 mV. This calibration allowed correction for a quadratic term in the nanovoltmeter response. Each $+--+$ measurement sequence took approximately 10 min to complete. The mean SNS-SIS difference for eighteen data sets was 0.5 nV with a type A standard uncertainty (1 s.d.) in the mean of 1.1 nV.

Finally, we measured the linearity of a digital voltmeter (DVM) to demonstrate the full range and utility of the new programmable standard. The array voltage was applied to the DVM where it was integrated for 3 s on the 1 V range. For a 16.000 000 GHz drive frequency, the smallest voltage increment was 4.234 923 3 mV. Figure 3 shows the deviation from linearity of the DVM at each of the 513 different voltages between $-1.084\,140\,4$ and $+1.084\,140\,4$ V. The 28 min total measurement time was limited by the DVM integration time. The ability to digitally select the array step voltage and to be certain that there are no spontaneous transitions between steps makes this measurement much faster and simpler than would be the case using a conventional SIS voltage standard.

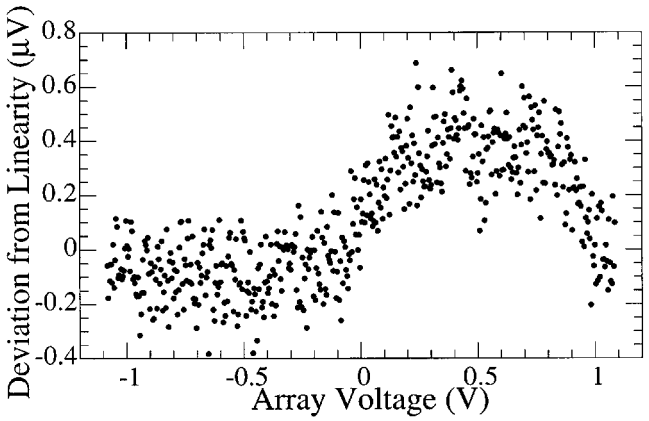

FIG. 3. Deviation from linearity of a digital voltmeter.

In conclusion, we have demonstrated a new Josephson voltage standard that can be programmed in less than 1 μs over the voltage range from -1.08 to $+1.08$ V. We have shown that the output voltage is stable and accurate by comparing it to a conventional SIS voltage standard. The two standards agreed within 0.5 nV with an uncertainty of 1.1 nV. We demonstrated the programmability of the standard by measuring the linearity of a DVM at 513 points over the range from -1.08 and $+1.08$ V. This SNS programmable voltage standard will find application where inherent stability and fast programmability are required.

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