Quasi-TEM Model for Coplanar Waveguide on Silicon

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***Abstract*- This paper compares a simple quasi-TEM model for coplanar waveguide fabricated on moderately doped silicon substrates to measurement. While the coplanar waveguide currents and magnetic fields are unaffected by the substrate, a simple capacitive model can accurately account for the effects of the substrate.**

INTRODUCTION

We apply the calibration comparison method [1], [2] to directly measure the resistance *R*, inductance *L*, capacitance *C*, and conductance *G* per unit length of coplanar waveguide (CPW) fabricated on silicon substrates and show that the model of Fig. 1 accurately determines *C* and *G*.

Kwong, et al. [3], Seguinot, et al. [4], and Ko, et al. [5] have proposed closed-form expressions for analyzing CPW on silicon substrates. However the analysis of [3] requires some finite-difference calculations, the models of [3] and [4] neglect the capacitance through the silicon substrate, and Williams, et al. [6] point out some difficulties in the analysis of [5]. Here we compare to measurement the model of Fig. 1, which is based on closed-form expressions from [3], [5], [7], and [8] and accounts for substrate capacitance, conductance, and fringing fields.

MEASUREMENT PROCEDURE

Reference [2] showed how to use the calibration comparison method [1] to accurately determine the inductance *L*, capacitance *C*, resistance *R*, and conductance *G* per unit length of printed transmission lines. A multiline thru-reflect-line (TRL) calibration [9] measures the line's propagation constant γ directly. A comparison of this calibration, whose reference impedance is equal to the characteristic impedance Z_0 of the transmission line [10], to a multiline TRL reference calibration with reference impedance correction [11] determines Z_0. Then *L*, *C*, *R*, and *G* are found from $R+j\omega L \equiv \gamma Z_0$ and $G+j\omega C \equiv \gamma/Z_0$.

In this work we apply this method to CPW fabricated on moderately doped silicon substrates using CPW reference lines fabricated on semi-insulating gallium arsenide. These reference lines had a metal thickness *t* of 0.5 µm and center conductor width *w* of 73 µm separated from two ground planes of width w_g=250 µm by gaps of width *s*=49 µm.

INDUCTANCE AND RESISTANCE

We first investigated the *L*, *R*, *C*, and *G* per unit length of the three CPWs of [2] fabricated directly on silicon substrates. These CPW conductors were formed by evaporating a thin titanium adhesion layer followed by approximately 0.5 µm of gold directly on three different silicon substrates. To assure the maximum measurement accuracy, [2] used the same metal geometries and metal thickness as the reference wafer.

Figure 2 of [2] compared *L* and *R* for these CPWs to that of the CPW fabricated on the semi-insulating gallium arsenide reference wafer and showed that *R* and *L* were insensitive to changes in the substrate. This indicates that the magnetic fields in the CPW are not affected by these moderately doped substrates: the currents are still confined to the metals.

CAPACITANCE AND CONDUCTANCE

Figure 2 shows the capacitance *C* and conductance *G* per unit length of the CPW measured in [2]: this figure shows that *C* and *G* are changed by the substrate parameters. It also compares the measurements of *C* and

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G to the results of the simple quasi-TEM model of Fig. 1 and shows good agreement. This model attributes C and G to the properties of the silicon substrate and the thickness and dielectric constant of the native oxides or depleted regions between the metals and the silicon substrate: the models of [3] and [4], which neglect the substrate capacitance, underestimate the measured capacitances significantly. The close agreement of this simple quasi-TEM model with the measurements also indicates that the interaction of the electric fields with the lossy silicon substrate has not given rise to any significant non-TEM phenomena.

We determined all of the parameters of the closed form model from direct measurement, approximate manufactures specifications, and material parameters found in the literature. On the 300-500 Ω·cm and the 140 Ω·cm substrates we left a native oxide on the silicon surface before metal deposition. Here we set $\rho_s=1/\sigma_s=400$ Ω·cm and 110 Ω·cm, consistent with the approximate specifications from the manufacturer, $\epsilon_i=3.9\epsilon_0$ and h_i equal to 0.005 μm and 0.0037 μm, the measured oxide thicknesses. For the CPW on the 2-5 Ω·cm p-type substrate we removed the native oxide. Here we set $\rho_s=1/\sigma_s=3.6$ Ω·cm and $\epsilon_i=11.7\epsilon_0$ and h_i = 0.44 μm, the calculated depletion depth at the metal-semiconductor interface.

CPW With Thick Passivation

We also fabricated CPWs with $w = s = 10$ μm, 5 μm, and 2 μm on a thick oxide layer grown on 135 Ω·cm silicon substrate. These lines had a metal thickness t of 2 μm; we assumed that the relative dielectric constant of the 6 μm thick oxide layer and 4 μm thick passivation layer was 3.9, reasonable for these SiO_2 layers. Figure 3 shows that the C and G predicted by the model for $w = s = 10$ μm with and without the thick passivation layer compare well to the measured values; agreement for the other cases was similar.

Conclusion

We studied a number of CPWs fabricated on silicon substrates. Neither R nor L was affected by the substrate, perhaps because the substrate conductivity was not too high [3]. This result indicates that the currents and the magnetic field solutions correspond to those of a CPW on a low-loss dielectric. Although C and G were shown to depend on the substrate parameters, they were well described by a simple capacitive quasi-TEM model: no non-TEM phenomena were required in the description. The model investigated here accounts for substrate capacitance and, unlike the models of [3] and [4], estimates the measured CPW capacitance accurately; its ability to account for the capacitance of the passivation layer suggests that it could be used to estimate its dielectric constant.

Acknowledgments

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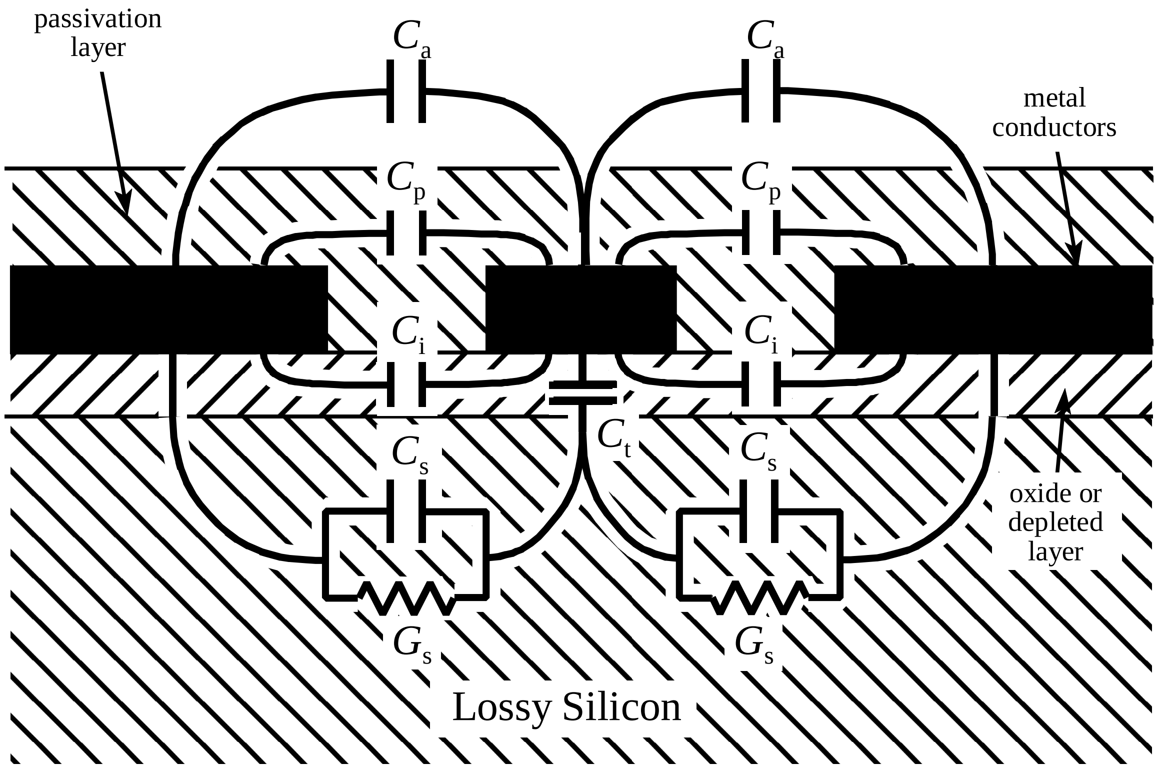

$$C_a = \epsilon_0 \left[F(w,s,w_g,t) - F(w',s',w_g,t) \right] \; ; \; C_p = \epsilon_p F(w',s',w_g,t)$$

$$w' \equiv 2 \sinh\left(\frac{\pi w}{4 h_p}\right) \; ; \; s' \equiv \sinh\left(\frac{\pi (s + w/2)}{2 h_p}\right) - \frac{w'}{2}$$

$$C_t = \epsilon_i \frac{w}{h_i} \; ; \; C_i = \epsilon_i F(w'',s'',0,0)$$

$$C_s = \epsilon_s F(w,s,w_g,0) \; ; \; G_s = \sigma_s F(w,s,w_g,0)$$

$$w'' \equiv 2 \sinh\left(\frac{\pi w}{4 h_i}\right) \; ; \; s'' \equiv \sinh\left(\frac{\pi (s + w/2)}{2 h_i}\right) - \frac{w''}{2}$$

Fig. 1. The capacitive model used in this work. Here w is the center conductor width, s the gap width, w_g the ground-plane width, t the metal thickness, h_i and ϵ_i the thickness and permitivity of the lower oxide or depleted layer, and h_p and ϵ_p the thickness and permitivity of the passivation layer. The expression for $F(w,s,w_g,t)$ is given in (1) of [8]. The expressions for w' and s' are taken from [7].

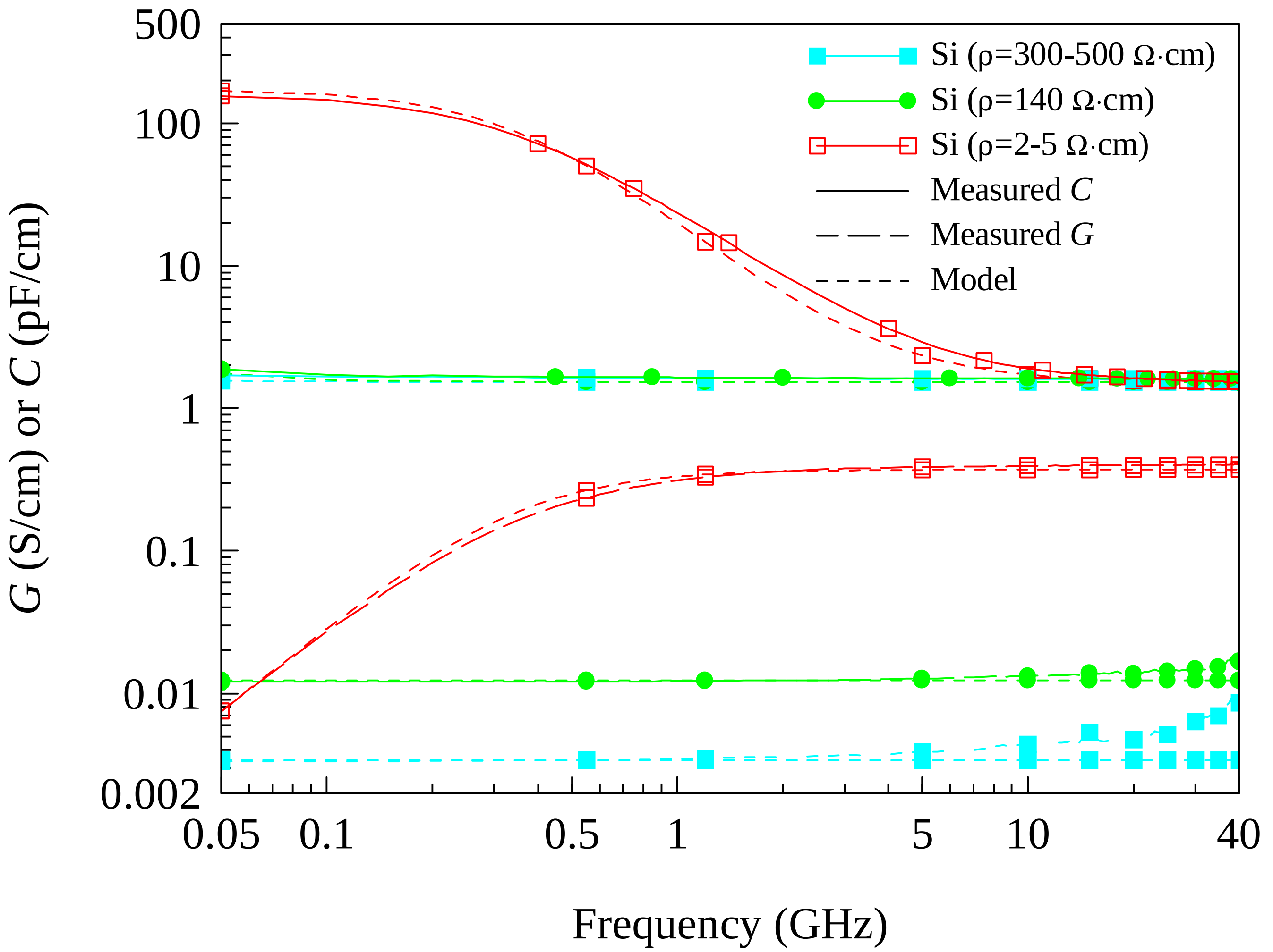

Fig. 2. The modeled and measured *C* and *G* for three CPWs fabricated directly on silicon. (Measurements from [2].)
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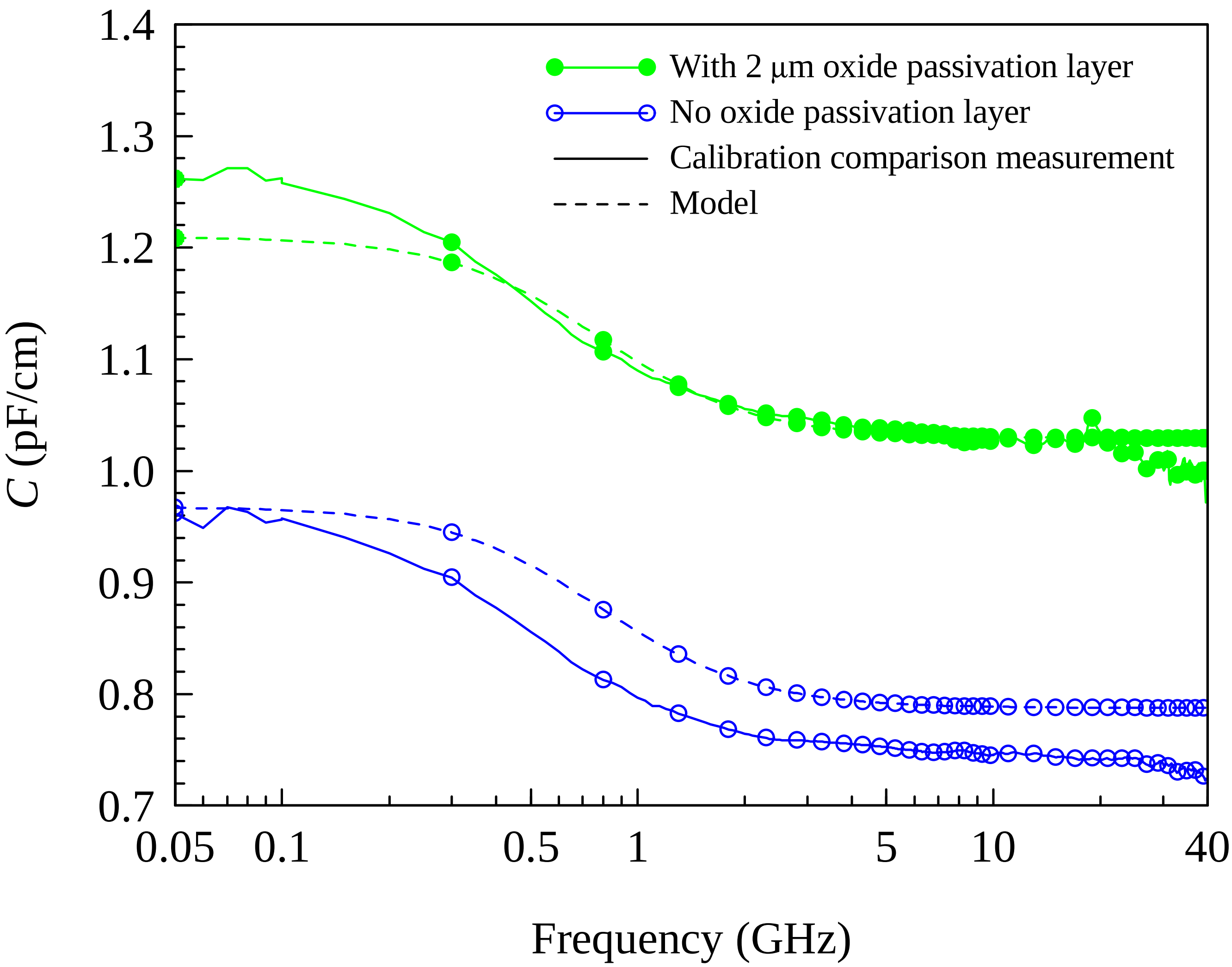

Fig. 3. The modeled and measured *C* of CPW with and without a thick SiO_2 passivation layer. c:\htb386\CPWmodel\Janezic_TI\sio50_c.plt